Dual Output DC/DC Controller Combines Digital Power System Management with Analog Control Loop for ±0.5% V_{OUT} Accuracy

Gregory Manlove

Though power management is critical to the reliable operation of modern electronic systems, voltage regulators are perhaps the last remaining "blind spot" in today's digitally managed systems. Few regulators have the means for direct configuration or monitoring of key power system operating parameters. As a result, power designers who want complete digital control must use a mixed bag of sequencers, microcontrollers and voltage supervisors to program basic regulator start-up and safety functions. Digitally programmable DC/DC converters are available, most notably those with VID output voltage control designed for VRM core power supplies, but these specifically targeted converters do not directly communicate important operating parameters, such as real-time currents.

The LTC®3880/-1 solves the problem of complex power system management by combining a dual output synchronous step-down DC/DC controller with a comprehensive power management feature set accessed via the I²C-based PMBus. PMBus can be used to set the output voltage, margin voltages, switching frequency, sequencing and a number of other operating parameters (see "PMBus Control" below).
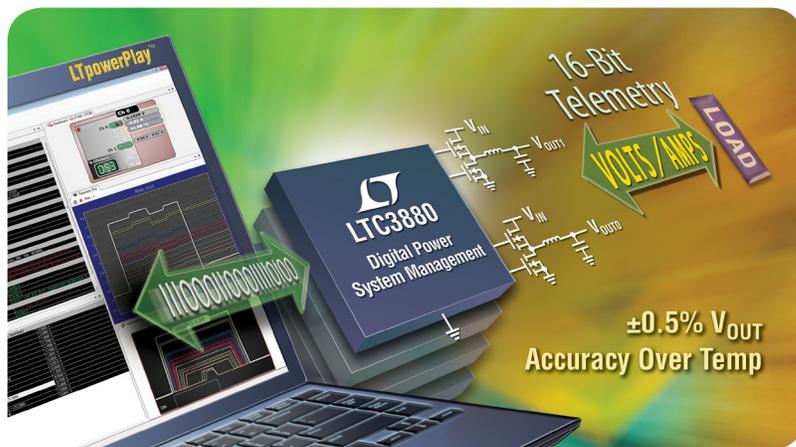
The LTC3880 in a digitally managed power system.

Linear in the News

In this issue...

LINEAR TECHNOLOGY ACQUIRES DUST NETWORKS: EXTENDS WIRELESS SENSOR NETWORKING CAPABILITIES

Linear Technology has announced the acquisition of Dust Networks, Inc., a leading provider of low power wireless sensor network (WSN) technology. The acquisition of Dust Networks enables Linear to offer a complete high performance wireless sensor networking solution. Dust Networks' low power radio and software technology complements Linear's strengths in industrial instrumentation, power management and energy harvesting technology.

Dust Networks' proven, low power wireless sensor network technology extends Linear's product portfolio into key growth areas in industrial process control, data acquisition and energy harvesting in applications where measurement of physical parameters has traditionally been impractical or impossible.

With the growing importance of machine-to-machine communications to enable remote data acquisition, low power wireless sensing is an emerging solution for many end-markets, including industrial process control, building automation and data center energy management.

Dust Networks pioneered SmartMesh® networks that comprise a self-forming mesh of nodes, or "motes," which collect and relay data, and a network manager that monitors and manages network performance and sends data to the host application. This technology is now the basis for a number of seminal networking standards. Dust Networks' technology combines low power, standards-based radio technology, time diversity, frequency diversity and physical diversity—to assure reliability, scalability, wire-free power source flexibility and ease-of-use. All motes in a SmartMesh network—even the routing nodes—are designed to run on batteries for years, allowing ultimate flexibility in placing sensors exactly where they need to go with low cost "peel and stick" installations.

Dust Networks' customers range from the world's largest industrial process automation and control providers such as GE and Emerson, to innovative, green companies such as Vigilent and Streetline Networks. Dust Networks' technology is found in a variety of monitoring and control solutions, including data center energy management, renewable energy, remote monitoring and transportation.

For more information, visit www.dustnetworks.com.

BEST ELECTRONIC DESIGN AWARD FOR BATTERY STACK MONITOR

Electronic Design magazine announced that Linear Technology's LTC6803 battery stack monitor is the winner of the Best Electronic Design award in the Automotive category.

Linear Technology's family of multicell, high voltage battery stack monitors are complete battery monitoring ICs that include 12-bit ADCs, precision voltage references, a high voltage input multiplexer and a serial interface. Multiple LTC6803 devices can be connected in series, without opto-couplers or isolators to enable monitoring of every cell in a long string of series-connected batteries. Applications include electric and hybrid electric vehicles, high power portable equipment, battery backup systems, and high voltage data acquisition systems.

ENERGY HARVESTING AND μMODULE PRODUCTS NAMED ELEKTRA AWARD FINALISTS

Electronics Weekly in the UK has selected two Linear Technology products as finalists for the Elektra European Electronics Industry Awards. The LTC3105 400mA synchronous step-up DC/DC converter for energy harvesting is a finalist for the Renewable Energy Design Award.

The LTC3105 incorporates maximum power point control (MPPC) and starts up with inputs as low as 250mV. Because the

LTC3105 can operate over an extremely wide input range of 0.225V to 5V, it is ideal for harvesting energy from high impedance alternative power sources, including single, dual or multiple photovoltaic cells, thermoelectric generators (TEGs) and fuel cells. The LTC3105 is ideally suited to power wireless sensors and data acquisition applications.

A second Linear Technology product, the LTM®4611 μModule® switch mode DC/DC regulator is a finalist for Power System Product of the Year. It is a complete switchmode DC/DC system-in-a-package point-of-load regulator, capable of generating its own 5V N-channel MOSFET gate drive for very efficient voltage conversion from 3.3V or less to loads as low as 0.8V at up to 15A.

Applications include systems with only 3.3V, 2.8V or 2.5V as the main power bus such as in very compact data storage and RAID systems, ATCA and networking cards, as well as medical and industrial equipment.

ANALOG CIRCUIT DESIGN BOOK IN SECOND PRINTING

The 960-page hardcover book, *Analog Circuit Design: A Tutorial Guide to Applications and Solutions*, edited by Bob Dobkin and Jim Williams, sold out of its first printing in only three weeks. The good news is that the publisher, Elsevier Science & Technology Books, expedited a second printing so you can now order the book from either Elsevier or Amazon.

For more information, or to purchase the book, go to www.linear.com/designtools/acd_book.php.

Electronic Design magazine announced that Linear Technology's battery stack monitor is the winner of the Best Electronic Design award in the Automotive category.

CONFERENCES & EVENTS

APEC 2012 (The Applied Power Electronics Conference & Exposition), Disney's Coronado Springs Resort, Orlando, Florida, February 5-9, Booths 1100 & 132—Linear will showcase its latest power products, including the LTC3300 for bidirectional multicell battery balancing, LTC4000 high voltage high current controller for battery charging and power management and LTC6803 multicell battery stack monitor. Sam Nork, Director of Linear's Boston Design Center, will make a presentation on "Active Cell Balancing" featuring the LTC3300 on Wednesday, February 8 at 10:30 AM as part of Session 5 in Fiesta 1/2. More info at www.apec-conf.org

Advanced Automotive Battery Conference (AABC) 2012, Omni Orlando Resort, Orlando, Florida, February 6-10, Booths 700 & 601—Linear will show its LTC3300 for bidirectional multicell battery balancing, LTC4000 high voltage high current controller for battery charging and power management, LTC6803 multicell battery stack monitor and LTC4366 high voltage surge stopper with overcurrent protection. More info at www.advancedautobat.com

CAR-ELE JAPAN 2012, Tokyo Big Sight, Tokyo, Japan, January 18–20, Booth West 12-45—Linear will show automotive-related products, including the LTC6803 battery stack monitor and LTM288x isolated μModule receivers + power. More info at www.car-ele.jp/en

Electronica China 2012, Shanghai New International Trade Fair Center, Shanghai, China, March 20-22, Hall W3, Booth 3312—Linear will show its LTM460x and LTM8047/8048 μModule power families, LTC4270/4271 Power over Ethernet devices for PoE+, LTC4000/LTC3300 battery chargers, unrestricted high speed ADCs, LTC6803 battery stack monitor, energy harvesting products, TimerBlox® devices and LED drivers. More info at www.electronicachina.com ∎

A principal benefit of digital power system management is reduced design cost and faster time to market. The LTC3880/-1 greatly simplifies the design of complex multirail systems with the free, downloadable LTpowerPlay™ software, a comprehensive PC-based development environment.

(LTC3880, continued from page 1)

The LTC3880 also allows monitoring of the supplies via a 16-bit data acquisition system, which supplies digital read back of input and output voltages and currents, duty cycle and temperature, including peak values of important parameters. The LTC3880 also includes extensive fault logging capability via an interrupt flag along with a nonvolatile memory, "black box" recorder, which stores the state of the converter's operating conditions immediately prior to a fault.

A principal benefit of digital power system management is reduced design cost and faster time to market. The LTC3880/-1 greatly simplifies the design of complex multirail systems with the free, downloadable LTpowerPlay™ development software, a comprehensive PC-based development environment (see Figure 6). In-circuit testing (ICT) and board debug require only a few clicks of the mouse—no need to solder in "white wire" fixes. The results of your design are immediately accessible, thanks to the availability of real-time

telemetry data, making it possible to predict power system failures and immediately implement preventive measures.

Perhaps most significantly, DC/DC converters with digital management functionality allow designers to develop green power systems that optimize energy usage while meeting system performance targets (compute speed, data rate, etc.). Optimization can be implemented at the point of load, at the board, rack and even at installation levels, reducing

Figure 1. Dual output regulator using external power MOSFETs

D0, D1: CMDSH-3TR
C_OUT0, C_OUT1: C330µF SANYO 4TPF330ML PLUS 2× 100µF AVX 12106D107KAT2A
L0, L1: VISHAY IHLP-4040DZ-11 1µH, 0.56µH
M1, M2: RENESAS RJK0305DPB
M3, M4: RENESAS RJK0330DPB

ANALOG CONTROL LOOP

ANALOG
CURRENT
WAVEFORM

FIXED f$_{SW}$

DIGITAL CONTROL LOOP

DIGITAL
RAMP

FIXED f$_{SW}$
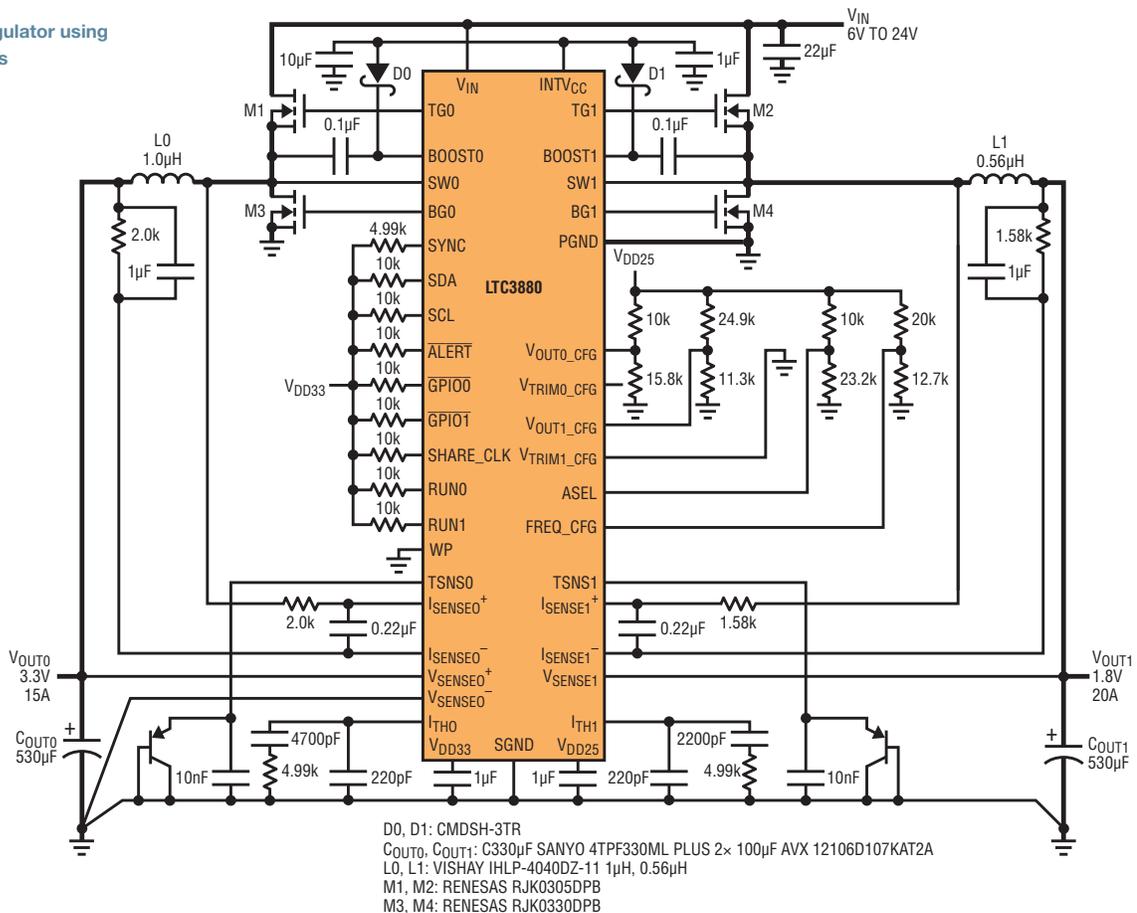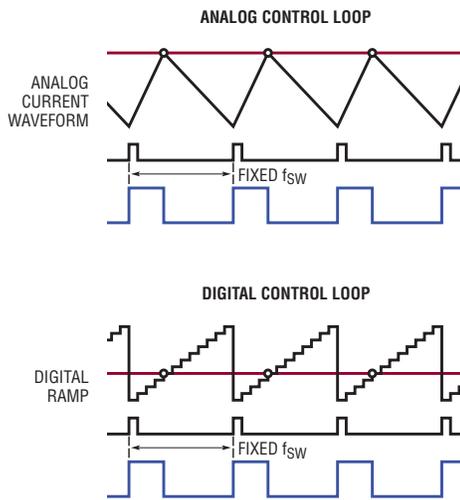
Figure 2. The LTC3880's analog control loop vs a digital control loop

ANALOG CONTROL LOOP

DIGITAL CONTROL LOOP

V$_{OUT}$
100mV/DIV
(AC-COUPLED)

205mV

I$_{OUT}$
10A/DIV
(15A LOAD STEP)

100µs/DIV

200µs/DIV

C$_{OUT}$ = **2 × 330µF** (POSCAP, 9mΩ) + 2 × 100µF

C$_{OUT}$ = **4 × 330µF** (POSCAP, 9mΩ) + 2 × 100µF

Figure 3. Comparative responses of analog and digital control loops to a 15A transient load step. The analog control loop requires only half the output capacitance of the digital loop while producing far superior settling times.

infrastructure costs and the total cost of ownership over the life of the product.

To provide best performance regulation, the LTC3880 sticks to a precision reference and temperature-compensated *analog* current mode control loop to produce a tight ±0.5% DC output voltage accuracy. The analog control loop makes for easy compensation, which is calibrated to be independent of operating conditions, yields cycle-by-cycle current limit, and produces a fast and accurate response to line and load transients—without any of

the ADC quantization-related errors found in products utilizing digital control.

The LTC3880 features an on-chip regulator for increased integration, whereas the LTC3880-1 allows for an external bias voltage for highest efficiency. Both parts are available in a thermally enhanced 6mm × 6mm QFN-40 package with either a −40°C to 105°C operating junction temperature range (E-grade) or a −40°C to 125°C operating junction temperature range (I-grade).

ANALOG CONTROL LOOP ENSURES BEST-IN-CLASS REGULATOR PERFORMANCE

The LTC3880/-1 is digitally programmable for numerous functions including the output voltage, current limit set point, and sequencing. The control loop, though, remains purely analog, which offers the best loop stability and transient response without the quantization effect of a digital control loop. Figure 2 compares the ramp curves of a controller IC with an analog feedback control loop to one with a digital feedback control loop. The analog loop has a smooth ramp, whereas the digital loop has discrete steps that can result in stability problems, slower transient response, more required output capacitance in some applications and higher output ripple and jitter on the PWM control signals due to quantization effects.

In fact, when put up against a comparable IC with a digital control loop, the LTC3880's analog control loop using 50% less output capacitance has better stability with a shorter settling time. Additionally, the digital control transient response has an oscillation prior to settling, due to the quantization effects caused by its finite ADC resolution. Figure 3 shows the transient response of the LTC3880's analog control loop compared to that of

Figure 4. It's easy to set up a complete development platform with LTpowerPlay software
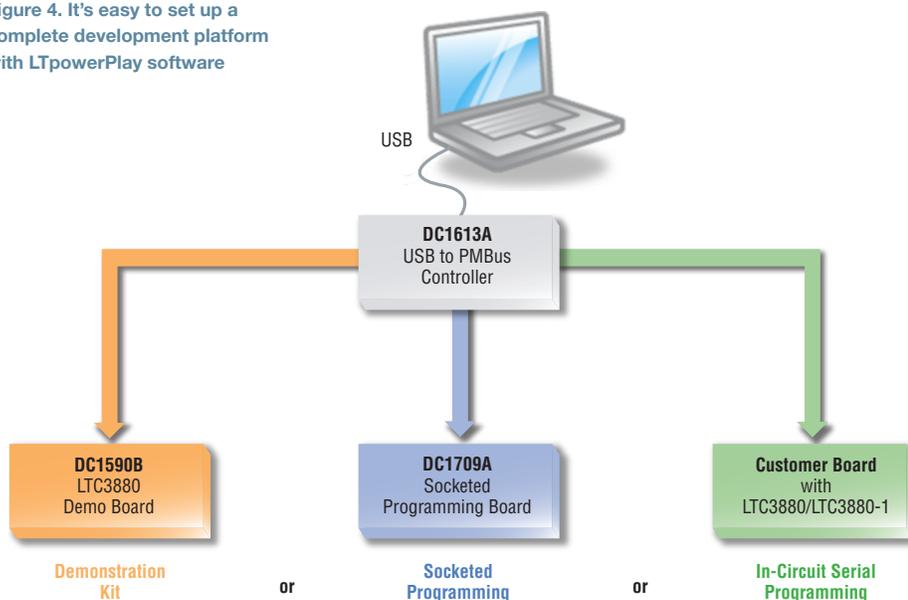
USB

DC1613A
USB to PMBus
Controller

DC1590B
LTC3880
Demo Board

DC1709A
Socketed
Programming Board

Customer Board
with
LTC3880/LTC3880-1

Demonstration
Kit

or

Socketed
Programming

or

In-Circuit Serial
Programming

Configurations are downloaded to internal EEPROM via the I²C serial interface supported by Linear Technology's LTpowerPlay PC-based development software. After the configuration file is stored on-chip in nonvolatile memory, the controller powers up autonomously without burdening the host.

a competitor's digital control loop. Note that the LTC3880 yields cleaner results with approximately half the output capacitance of the digital controller.

The LTC3880 is designed so the loop gain does not change when its configuration file is modified. When the output voltage or the current limit is modified, the transient response is unaffected and the compensation loop needs no adjustment.

PMBus CONTROL

The LTC3880/-1 features digital programming and read back for real-time control and monitoring of critical point-of-load converter functions. Configurations are downloaded to internal EEPROM via the I²C serial interface supported by Linear Technology's LTpowerPlay PC-based development software. Figure 4 shows the LTpowerPlay development platform with a USB to I²C/SMBus/PMBus adapter. After the configuration file is stored on-chip in nonvolatile memory, the controller powers up autonomously without burdening the host. Configuring a board is a simple task that requires zero firmware development.

PMBus functions include the ability to program specific power supply management parameters including:

- output voltage and margin voltages
- temperature-compensated current limit threshold based on inductor temperature
- switching frequency
- overvoltage and undervoltage high speed supervisor thresholds
- output voltage on/off time delays
- output voltage rise/fall times
- input voltage on/off thresholds
- output rail on/off
- output rail margin-hi/margin-lo
- responses to internal/external faults
- fault propagation

In addition, PMBus functions allow monitoring of power supply operation including:

- output/input voltage
- output/input current
- internal die temperature
- external inductor temperature
- part status
- fault status
- system status
- peak output current
- peak output voltage
- peak internal/external temperature
- fault log status

Figure 5. LTpowerPlay and PMBus used to control 15 or more rails.
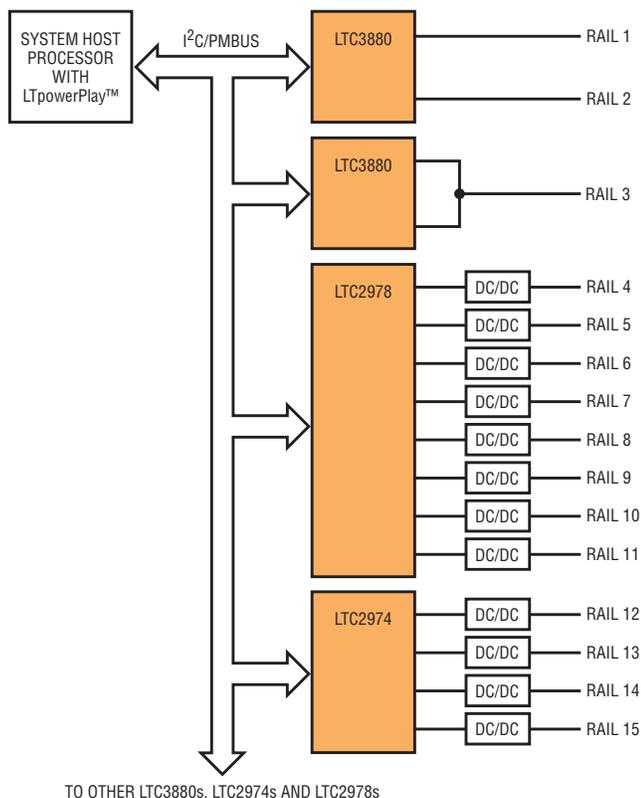
Linear Technology PMBus controllers such as the LTC3880 and companion ICs such as the LTC2978 make it easy to program power-up and power-down sequencing for any number of supplies. By using a time-based algorithm, users can dynamically sequence rails on and off in any order with simple programmable delays.
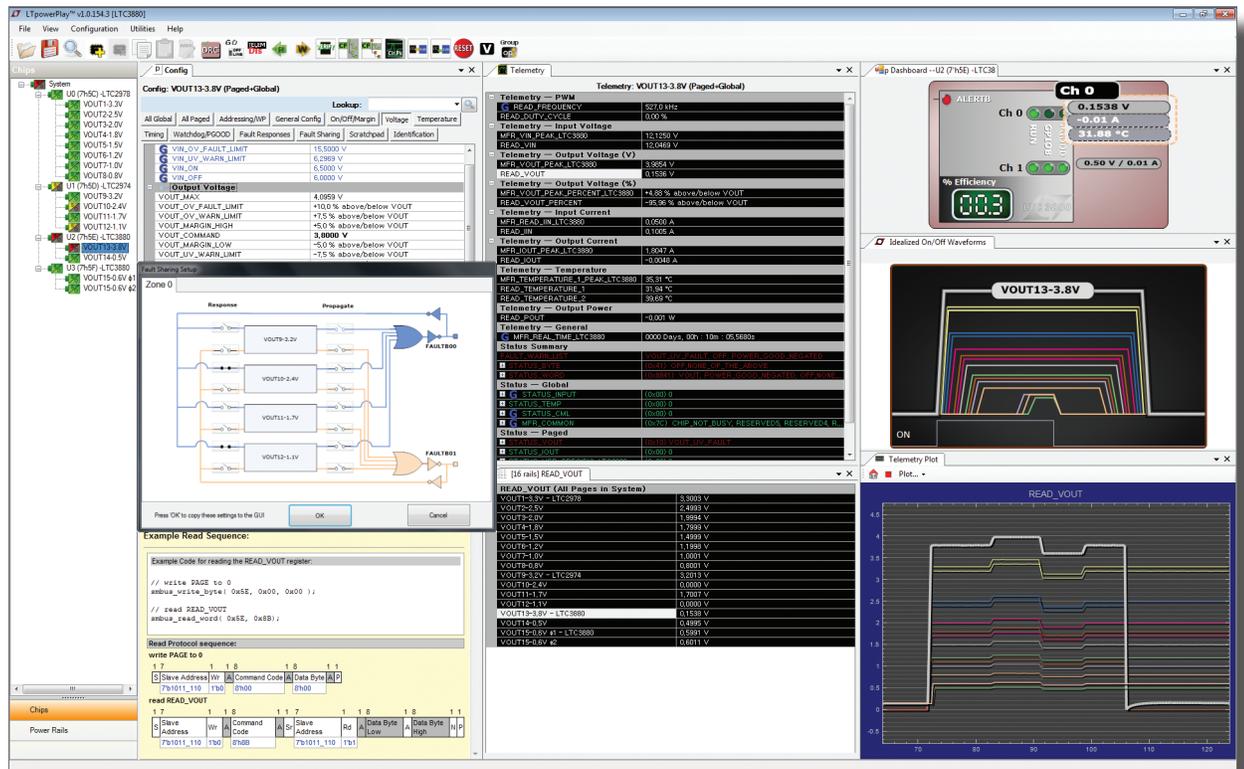

Figure 6. Complex, multirail power systems simplified. LTpowerPlay puts complete power supply control at your fingertips.

PUTTING TOGETHER A MULTIRAIL SYSTEM

A large multirail power board is normally composed of an isolated intermediate bus converter, which converts 48V, 24V or other relatively high voltage from the backplane to a lower intermediate bus voltage (IBV), typically 12V, which is distributed around a PC card.

Individual point-of-load (POL) DC-DC converters step down the IBV to the required rail voltages, which normally range from 0.5V to 5V with output currents ranging from 0.5A to 120A. Figure 5 shows how a multi-rail system can be controlled with various Linear Technology controllers and DC/DC converters PMBus devices. The

point of load DC/DC converters can be self-contained modules, monolithic devices or solutions comprising DC/DC controller ICs, associated inductors, capacitors and MOSFETs. These rails normally have strict requirements for sequencing, voltage accuracy, overcurrent and overvoltage limits, margining and supervision.

The sophistication of power management is increasing. It is not uncommon for circuit boards to have over 30 rails. These boards are already densely populated so adding digital power system management circuitry must require minimal board space and external pins. The system must be easily modified by the user or a system host processor. The LTC3880 works

seamlessly with other Linear Technology PMBus supervisors, companion ICs and Linear Technology regulators for optimal control of complex boards. These systems operate autonomously after initial configuration or communicate with the host for command, control and to report telemetry.

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PMBus chips can be added later without having to worry about system constraints such as a limited number of connector pins. Multiple addresses are supported in PMBus allowing over 100 unique devices on the same I²C bus.

and one or more of the bidirectional general purpose IO ($\overline{\text{GPIO}}$) pins. This greatly simplifies system design because rails can be sequenced in any order. Additional PMBus chips can be added later without having to worry about system constraints such as a limited number of connector pins. Multiple addresses are supported in PMBus allowing over 100 unique devices on the same I²C bus.

Rail sequencing to the on state can be triggered in response to a variety of conditions. For example, the LTC3880 and LTC2978 can auto-sequence when the intermediate bus voltage exceeds a programmed threshold ($V_{IN(ON)}$). Alternatively, rail on sequencing can be initiated in response to the rising edge of the RUN/CONTROL pin. Rail on sequencing can also be initiated by a PMBus command.

The $\overline{\text{GPIO}}$ pins on the LTC3880 can be shared with fault pins from LTC PMBus companion ICs to control fault response dependencies between rails. For example the system can be configured such that a fault on one rail can initiate the shutdown of any number of rails. If the fault response is configured for "immediate off no retry" and a fault occurs, the host must take action for the rails to be restarted. Alternatively, if the fault response is set to "immediate off infinite retry" and a fault occurs, the rail attempts to power up autonomously with a user programmable delays in a hiccup mode. The fault response can also be set to "ignore," where the $\overline{\text{ALERT}}$ pin is pulled low in

response to a fault, to alert the host of an issue, but the power supply continues to deliver power to the load. The $\overline{\text{GPIO}}$ pins can also be configured as power good status pins or as the fast UV comparator output for event-based sequencing.

LTpowerPlay DEVELOPMENT SYSTEM
Control of the LTC3880 is fully supported by the LTpowerPlay PC-based software development system, which allows a designer to modify the configuration settings for all Linear Technology PMBus products in real time—no need to manually rewire the board. Figure 6 shows LTpowerPlay in action, controlling a number of functions for multiple devices, such as the output voltage, protection limits and on/off ramps. Some waveforms are displayed including the sequencing of multiple rails and telemetry plots. A fault condition is indicated with the offending rail in red and any affected rails in yellow.

LTpowerPlay is available as a free download at www.linear.com/ltpowerplay. LTpowerPlay works in conjunction with other Linear Technology controller and companion ICs in order to quickly and easily configure multiple rail power systems.

CONCLUSION
The LTC3880/-1 combines best-in-class analog switching regulators with precision data conversion and a flexible digital interface for unsurpassed performance. Multiple LTC3880s can be used with other LTC products to create optimized multi-rail digital power systems. All Linear Technology PMBus products are

supported by the easy-to-use LTpowerPlay software development system.

Digital control over analog power supplies enables designers to get their systems up and running quickly providing an easy way to monitor, control and adjust supply voltages, limits and sequencing. Production margin testing is easily performed using a couple of standard PMBus commands. Debug is also simplified because the rail status is communicated over the bus.

Power system data can be sent back to the OEM providing information about the power supplies health and energy consumption. If a board is returned, the fault log can be read to determine which fault occurred, the board temperature and the time of the fault as well as historical data leading up to the fault. This data can be used to quickly determine root cause, whether the system was operated outside of its specified operating limits, or to improve the design of future products. Power consumption data can be used to reduce overall power use in real time.

Digital power is a rapidly growing field driven by customer demand for ever more complex boards. The LTC3880 and other Linear Technology PMBus products work together to give flexible digital control to high performance supplies. Board designers now have the tools to streamline the process of bringing best-in-class performance quickly to market. ∎

Integer-N Synthesizer with Integrated VCO Yields Top Notch PLL Performance in a 4mm × 5mm Package

Michel Azarian

High data throughput requirements in high bandwidth communications systems make the phase purity of the local oscillator critical to reliable performance. One way to conserve space and cost in such systems is to use an IC that combines the PLL and the VCO without sacrificing signal quality. The LTC6946 does just that by integrating a world-class frequency synthesizer, a low phase noise VCO and top-shelf performance, allowing designers to meet stringent RF system performance goals.

LTC6946 SAVES TIME AND SPACE

In either an RF receiver or transmitter system, the local oscillator (LO) plays a key role in achieving the desired system specifications. The main goal in such systems is to maximize the signal-to-noise ratio (SNR) of the received or transmitted signal while limiting board space, power and cost.

There are several factors that limit the SNR in an RF system, including the linearity and noise figure of the receive or transmit chain, and the phase noise and spurs of the LO.

Proper component selection in the RF chain limits the linearity and noise figure degradation to a tolerable level. Similarly, careful design decisions must be made to attain the desired phase noise and spurious level of the LO.

High performance systems call for an LO source with high spectral purity, necessitating the use of a low in-band phase noise synthesizer with an external high end VCO. Such a solution requires a large amount of board space, an involved design process and is relatively expensive.

The LTC6946, in contrast, meets the requirements of high performance systems by integrating these components in a single 4mm × 5mm package. Specifically, it combines an industry-leading ultralow phase noise and spurious integer-N synthesizer with a low phase noise and broadband VCO. Overall costs are low compared to an external VCO system, and integrating the LTC6946 in an RF system is straightforward, as shown later in this article.

WHAT'S INSIDE THE LTC6946?

Figure 1 shows a simplified LTC6946 block diagram, along with the external reference clock (an OCXO, for example) and loop filter components.

In a nutshell, the phase/frequency detector (PFD) of Figure 1 compares the phase and frequency of the reference clock, f_{REF}, after its division by R to produce f_{PFD}, to those of the VCO following an integer division of N. The PFD then controls the current sources of the charge pump to ensure that the VCO runs at a rate such that when it is divided by N, its frequency is equal to f_{PFD} and its phase is in sync with the reference clock. This describes a negative feedback mechanism, with the external loop filter components stabilizing the loop and setting the control bandwidth. The O divider increases the output frequency range by dividing down the VCO output to create more frequency bands than just that of the VCO. The following equation relates the output frequency to f_{REF}.

$$f_{LO} = \frac{f_{REF}}{R} \bullet \frac{N}{O}$$

Figure 1. Simplified LTC6946 block diagram with external reference clock and loop filter
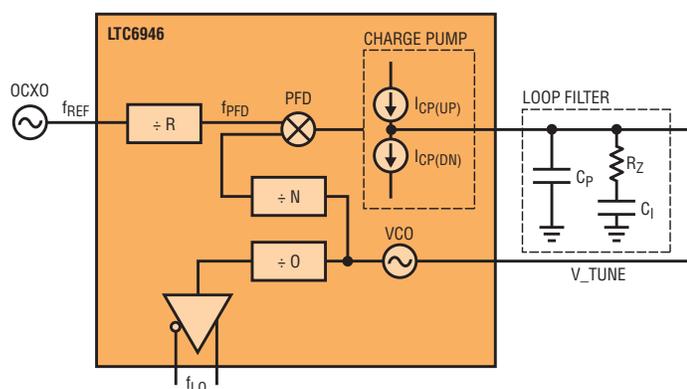
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Table 1. LTC6946 versions

	LTC6946-1	LTC6946-2	LTC6946-3
VCO Range (MHz)	2240 to 3740	3080 to 4910	3840 to 5790
f_{LO} (MHz) with O = 1	2240 to 3740	3080 to 4910	3840 to 5790
f_{LO} (MHz) with O = 2	1120 to 1870	1540 to 2455	1920 to 2895
f_{LO} (MHz) with O = 3	747 to 1247	1027 to 1637	1280 to 1930
f_{LO} (MHz) with O = 4	560 to 935	770 to 1228	960 to 1448
f_{LO} (MHz) with O = 5	448 to 748	616 to 982	768 to 1158
f_{LO} (MHz) with O = 6	373 to 623	513 to 818	640 to 965

LTC6946 VERSIONS

There are three different frequency range versions of the LTC6946, summarized in Table 1. All versions offer superior in-band phase noise, with industry-leading 1/f performance. The integrated VCOs achieve low phase performance and require no external components.

IMPORTANCE OF LOW PHASE NOISE

The impact of LO phase noise on a system can be illustrated with a simple down-converting receiver. Consider a perfect tone at a frequency f_{RF} downconverted by an ideal mixer with the use of a non-ideal LO source at f_{LO} as shown in Figure 2. The LO source is shown to have a practical phase noise profile illustrated by the surrounding skirts. As can be seen at the intermediate frequency (f_{IF}), the down-converted ideal tone is corrupted by the phase noise of the LO source.

The ideal tone present at the RF port of the mixer has infinite SNR, or a very large one as limited by the matching

system. The mixer, being ideal, does not degrade the quality of the received signal. However, the IF output of the mixer has a much lower SNR compared to the received signal due to the phase noise of the LO. This example presents a simple way for describing the importance of low phase noise in preserving signal quality.

Effect of Phase Noise on Digitally Modulated Signals

Complex digital modulation schemes make efficient use of limited channel bandwidth in wireless communications, but tend to put pressure on the phase noise requirements used to generate the LO in these systems. To further clarify the effect of phase noise on such an approach, assume that the RF port of the mixer in Figure 2 receives a 64-quadrature amplitude-modulated (64-QAM) signal. Figure 3 shows the IF signal constellation diagram, a 2-dimensional scatter plot of the demodulated signal at symbol sampling instants, assuming both the mixer and the LO source are ideal.

Because each of the dots is distinct and centered exactly within the decision boundary, a proper demodulation scheme will decipher the received message with zero errors.

Going back to the system given in Figure 2, and assuming the phase noise of the LO as the only non-ideal element in the system, the constellation of the IF signal becomes that shown in Figure 4.

The landing locations of the sampled symbols are skewed by the LO phase noise. Consequently, the symbols are not as easily intelligible by the demodulator. As such, phase noise alone is capable of making the demodulator's job tricky, causing errors in the interpreted message.

To put this into perspective, compare the effect of phase noise to that of white noise on the demodulator's ability to deduce the message correctly. Assume that the system and signals in Figure 2 are all ideal
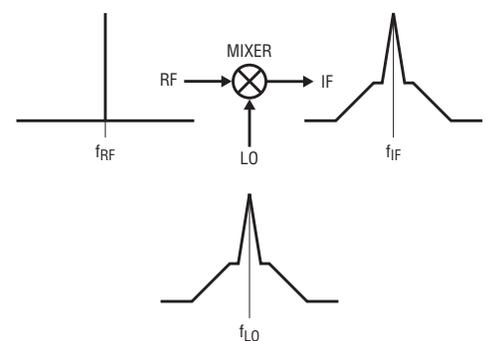

Figure 2. An ideal mixer downconverting an ideal tone with the use of a real-life LO

All LTC6946 versions offer superior in-band phase noise, with industry-leading 1/f performance. The integrated VCOs achieve low phase performance and require no external components.
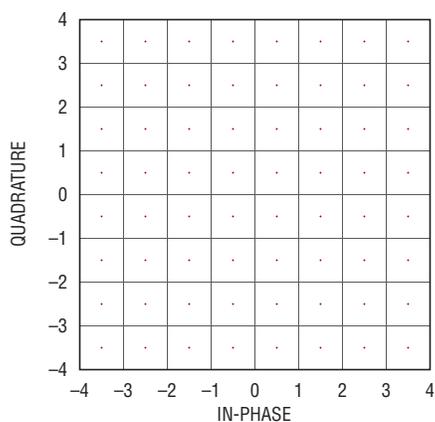

Figure 3. Ideal constellation of a 64-QAM signal
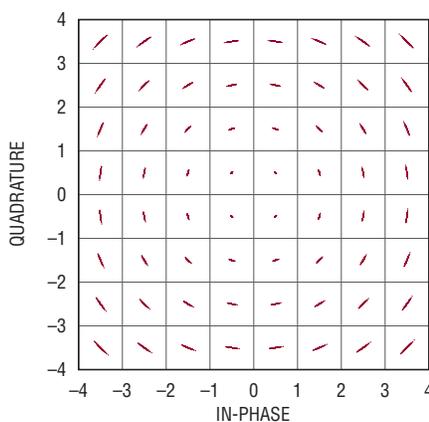
Figure 4. 64-QAM constellation corrupted by phase noise
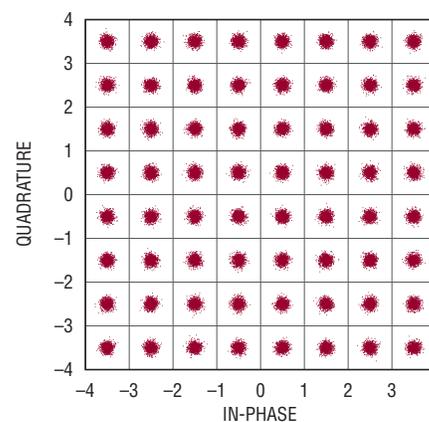
Figure 5. 64-QAM constellation corrupted by white noise

except that the mixer has a non-zero noise figure, such that it adds white noise to the received signal. The constellation of the IF signal in this case is shown in Figure 5.

Once again, the symbols are offset from their ideal spots, causing errors in the received signal. The ultimate consequence of white noise on the system is very similar to that of phase noise.

In a practical situation, the received signal at the RF port of the mixer has a limited SNR, which is already inadequate for error-free demodulation at the IF port. A real mixer worsens the situation due to its own impairments. The phase noise of the LO further harms the SNR if it is not carefully designed. Accordingly, the phase noise must stay at or below the level of SNR degradation acceptable in the system.

Effect of Phase Noise on Adjacent Channel

Another reason for requesting low phase noise is to avoid or reduce the effects of reciprocal mixing. It is common in communications systems with multiple channels in a certain band to have large variations in signal strength between two adjacent channels. If a weak signal located next to a much stronger adjacent channel is to be properly downconverted and demodulated, the LO used with the mixer must have low phase noise. It must be low enough to prevent the spectral leakage from the larger signal from seriously degrading the desired channel's SNR.

Assume that in Figure 2 two ideal tones are received at the RF port of the mixer and that the LO has the phase noise profile shown in the same figure. Figure 6 depicts the new system and illustrates reciprocal mixing.

As seen at the IF, the phase noise of the LO makes the stronger adjacent channel
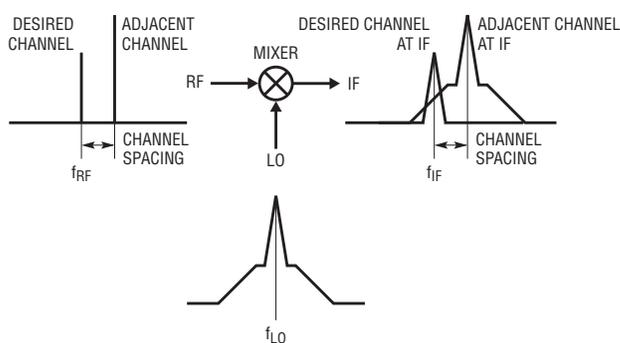
Figure 6. Reciprocal mixing due to LO phase noise

The LTC6946 has an industry leading –274dBc/Hz normalized in-band
1/f noise specification, which is equivalent to a –134dBc/Hz phase noise
level for a 100MHz reference clock at an offset of 100Hz. This number
challenges the best 100MHz crystal oscillators available on the market.

"leak" into the weaker desired one and severely limit its SNR. The same concepts apply whether the mixer is used to down-convert or upconvert the incoming signal.

THE ANATOMY OF PHASE NOISE AND LTC6946 PERFORMANCE
So how does the LTC6946 stack up against synthesizer performance metrics? To illustrate this, the phase noise profile of a given LO is subdivided into four approximate regions as one of the LO sidebands shows in Figure 7. It is assumed that this LO source is produced by a PLL IC that locks a high frequency VCO to a lower frequency reference clock. The performance of the LTC6946 in each distinct region is discussed.

Close-In
Close-in phase noise is ideally dominated by the phase noise profile of the reference clock. However, the flicker (or 1/f) noise of the PLL IC usually worsens the noise here. This region typically extends to 100s or 1000s of Hz from the LO. Close-in phase noise degrades the performance of complex communications schemes especially if they have long burst durations.

The LTC6946 has an industry leading –274dBc/Hz normalized in-band 1/f noise specification, which is equivalent to a –134dBc/Hz phase noise level for a 100MHz reference clock at an offset of 100Hz. This number challenges the best 100MHz crystal oscillators available on the market. As a result, and unlike other PLL ICs, the LTC6946 does not typically degrade the reference-dominated close-in phase noise.
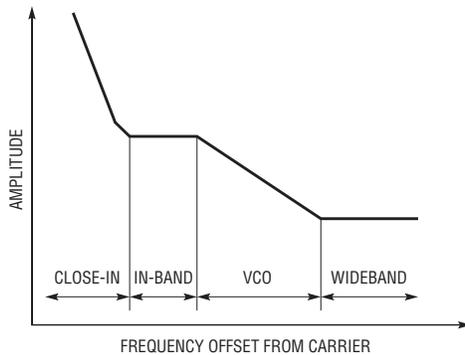
Figure 7. Single-sideband phase noise anatomy

In-Band
In-band phase noise is usually dictated by the PLL IC and any noisy components in the loop filter. The reference clock might also elevate the noise in this region if it is not properly chosen. The in-band phase noise region typically extends to around the loop bandwidth of the PLL. Depending on several factors, such as channel bandwidth and phase noise levels in the other regions, in-band phase noise

is often the most significant contributer to signal SNR degradation due to phase noise.

The LTC6946 boasts an impressive –226dBc/Hz normalized in-band phase noise floor that keeps the "plateau" area as low as possible. This figure allows the LTC6946 to be used in the most demanding applications.

VCO
VCO phase noise, as the name implies, is mainly contributed by the VCO. Depending on the PLL loop bandwidth and channel width, the VCO phase noise can be a significant contributor to signal SNR degradation due to phase noise. And, depending on the channel spacing, VCO phase noise might give birth to reciprocal mixing.

The VCOs integrated into the LTC6946 have competitive phase noise compared to standalone broadband VCOs, ensuring excellent overall performance.

Figure 8. Adjacent channel interference due to reference spurs
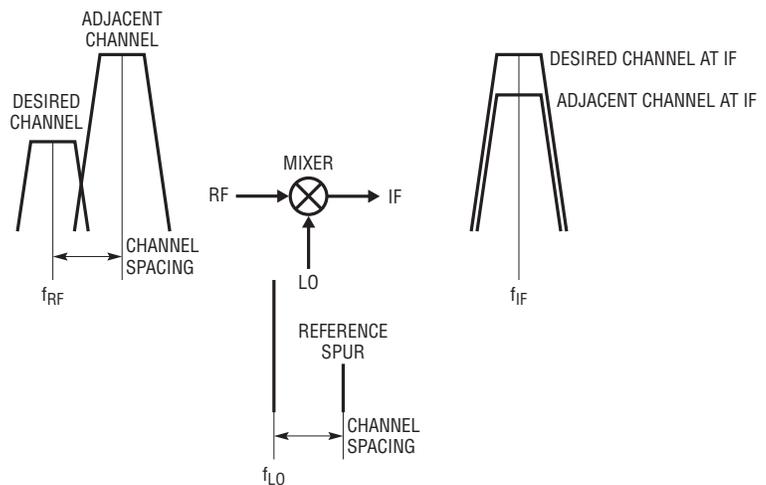
The LTC6946 boasts an impressive –226dBc/Hz normalized in-band phase noise floor that keeps the "plateau" area as low as possible. This figure allows use of the LTC6946 in the most demanding applications.

Wideband

Wideband phase noise is dominated by the buffering present at the output of the vco. Like vco noise, and due to reciprocal mixing, wideband phase noise affects adjacent channels. Even far out channels experience a rise in their noise floor due to a distant strong channel, commonly referred to as a blocker.

The LTC6946 has a superior –157dBc/Hz wideband phase noise floor that matches the performance of standalone broadband vcos, thus minimizng blocking effects.

THE IMPORTANCE OF LOW SPURS

An integer-N PLL produces spurs around the LO offset at its PFD update rate (f_{PFD}) and at the harmonics of this rate. These are commonly referred to as reference spurs.

Consider a typical scenario in a multi-channel wireless communications system that carries a stronger channel adjacent to the desired but weaker channel as shown in Figure 8. Only one of the LO reference spurs is shown.

In an integer-N PLL, f_{PFD} is usually chosen to be equal to the channel spacing, which means that the reference spurs are positioned at channel spacing from the LO. These spurs translate all adjacent and nearby channels to the center of the IF, along with the LO translating the desired channel to the same exact frequency.

These undesired channels, being uncorrelated to the signal in the desired channel, appear as an elevated noise floor to the desired signal and limit its SNR. Hence, it is important to keep reference spurs at bay.

LTC6946 DESIGN EXAMPLE

To appreciate the simplicity of the design process with the LTC6946, a complete design example for the LO of a wideband point-to-point radio for wireless access is shown here. The design assumes the following frequency plan.

• LO frequency band: 4700MHz to 5700MHz

• Frequency step size (channel-to-channel spacing): 5MHz

• Reference clock frequency: 100MHz

Based on the frequency ranges in Table 1, the LTC6946-3 is suitable for covering the requested frequency band. All further design choices can be made using the PLLWizard™ free PLL design and simulation tool found at www.linear.com/designtools/software.

Entering the given frequency information in PLLWizard and picking the approximate noise optimized loop bandwidth suggested by the PLLWizard tool produces the loop filter values needed to modify a DC1705A-C demo board. Since the LTC6946 vco gain is nearly constant as a percentage of the frequency, the loop filter designed at any frequency within the band works for all other frequencies. Figure 9 shows a snapshot of PLLWizard used in completing this design.

The DC1705A-C is updated with the loop filter components as found above and its schematic is shown in Figure 10.

Figure 11 verifies that the achieved phase noise matches that predicted by PLLWizard. Double-sideband integrated noise from 100Hz to 40MHz allows for

Figure 9. Snapshot of the PLLWizard software tool used in designing a broadband LO from 4700MHz to 5700MHz with 5MHz channel spacing

close to 40dB of SNR, sufficient to meet most demanding application requirements.
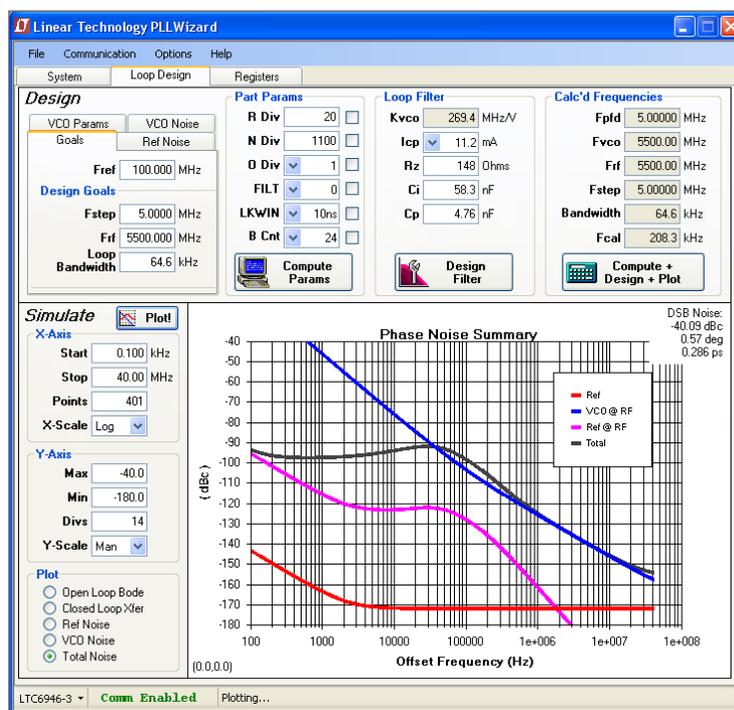
Figure 12 shows the spurious performance at 5500MHz. The tallest reference spurs are about –97dBc, which is phenomenal at an LO frequency this high, and are unlikely to contribute to any noticeable adjacent channel interference.

After following the quick and straightforward steps summarized above, the circuitry is ready to be deployed in a real-life point-to-point radio application.

CONCLUSION

The LTC6946 simplifies frequency synthesis by integrating an integer-N synthesizer with a VCO without sacrificing performance. It is ideal for many demanding applications where low phase noise is essential. To top it off, designing with the LTC6946 is a breeze when combined with the PLLWizard tool, available at www.linear.com/designtools/software. ∎
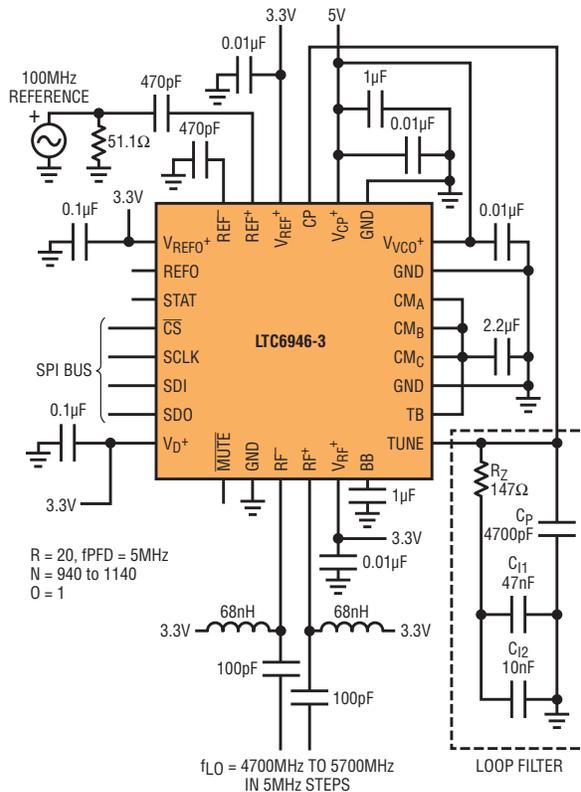
Figure 10. Schematic of the 4700MHz to 5700MHz LO synthesizer circuit
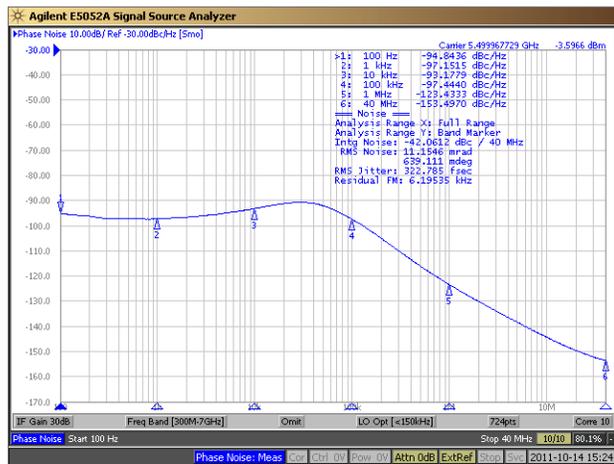
Figure 11. Phase noise at 5500MHz
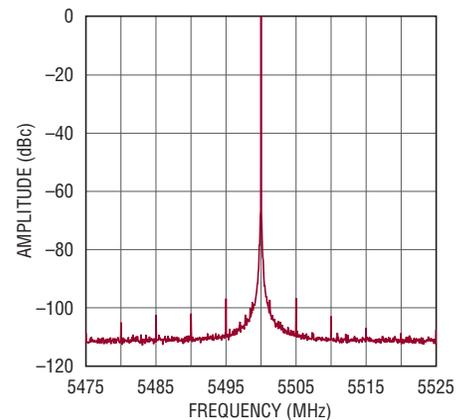
Figure 12. Spectrum at 5500MHz

Supercapacitor Charger and Ideal Diode for Power Supply Ride-Through Systems

George H. Barbehenn

Supercapacitors, capacitors with up to 100F of charge storage, are emerging as an alternative to batteries in applications where the importance of power delivery trumps that of total energy storage. Supercapacitors have a number of advantages over batteries that make them a superior solution when short term, high power is needed, such as in power ride-through applications. These advantages include lower effective series resistance (ESR) and enhanced durability in the face of repeated charging.

Like batteries, supercapacitors have some specialized application needs that make using a dedicated IC desirable.

Supercapacitor technology can now offer capacitors as large as 100F, but the maximum working voltage on these

capacitors is 2.7V or less. Because most systems require operating voltages higher than this, many supercapacitors are

Figure 1. Block diagram of the LTC4425
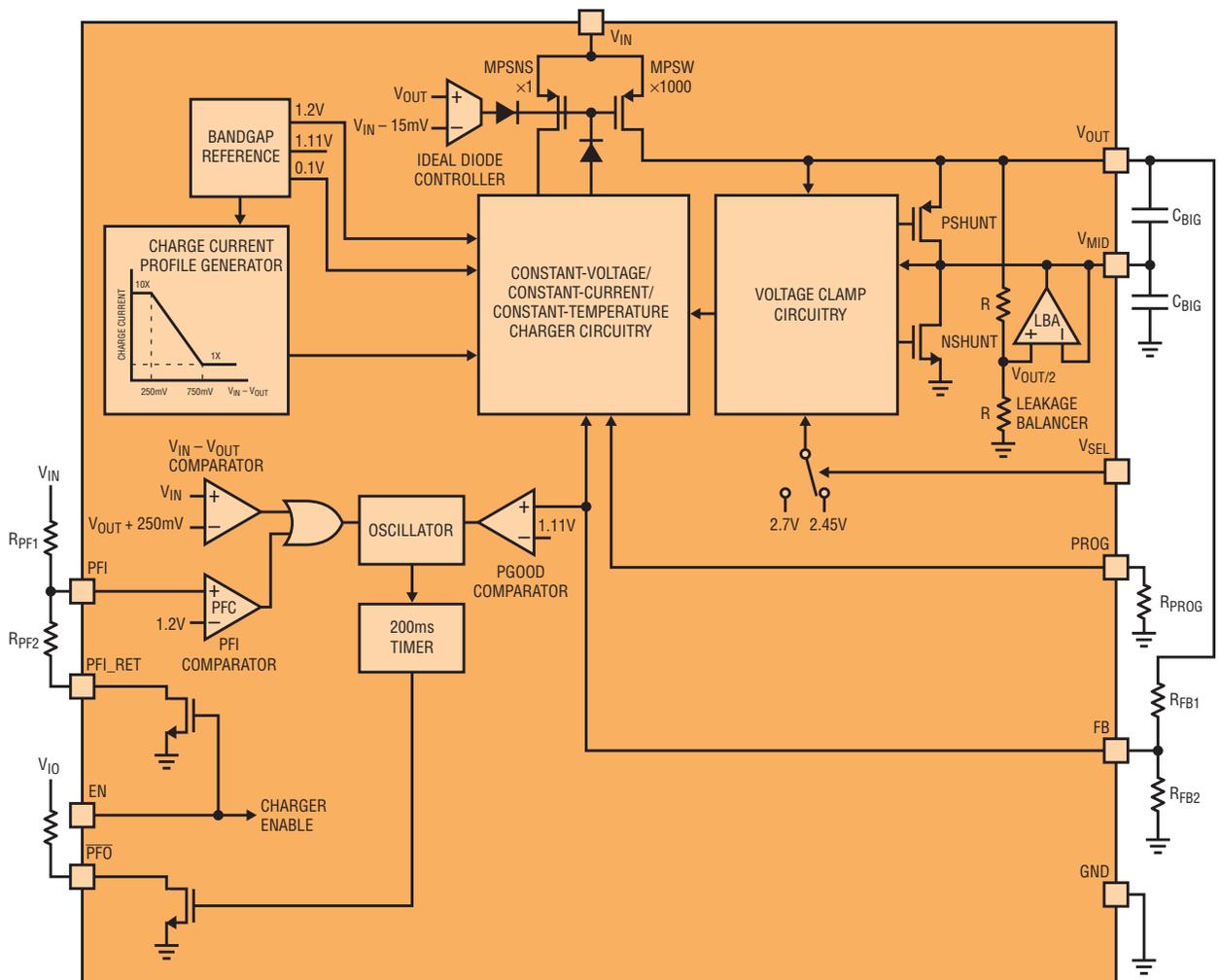
The maximum working voltage on a single supercapacitor is 2.7V or less. Because most systems require operating voltages higher than this, many supercapacitors are supplied as a pair of capacitors within a single, center-tapped package. The LTC4425 is designed to to charge stacked supercapacitors and provide a regulated output voltage for the system load.

supplied as a pair of capacitors within a single, center-tapped package. The LTC4425 is designed to charge two stacked supercapacitors and provide a regulated output voltage for the system load.

THE LTC4425 ARCHITECTURE

The LTC4425 has two modes of operation: Normal and LDO.

Normal Mode

In Normal mode, the LTC4425 can be thought of as an ideal diode with current limit and supercapacitor-specific functions (see Figure 1). If we ignore everthing but the ideal diode controller, MPSNS and MPSW, the LTC4425 behaves like an ideal diode. MPSW is turned on whenever v_{IN} is lower than v_{IN} by more than 15mV.

A fraction (1/1000) of the current in the v_{OUT} pin is impressed on the resistor attached to the PROG pin and the resultant voltage is compared to a reference voltage. When the voltage on the PROG pin reaches the reference voltage, no additional current is allowed to flow out of the v_{OUT} pin.

In Normal mode, the regulation function is not controlled by the output voltage alone, but by $v_{IN} - v_{OUT}$ (see Figure 2). Normal mode is selected by connecting the FB pin to v_{IN}. In Normal mode, as long as $v_{IN} - v_{OUT}$ is greater than 0.75V, the charge current is 1/10 the programmed value. As the $v_{IN} - v_{OUT}$ voltage decreases from 0.75V to 0.25V, the charge current increases linearly to the programmed value at $v_{IN} - v_{OUT}$ = 0.25V. For $v_{IN} - v_{OUT}$ voltages less than 0.25V, but greater than 15mV, the v_{OUT} current is $1000/R_{PROG}$, and can be as high as 2A. However, the MPSW device
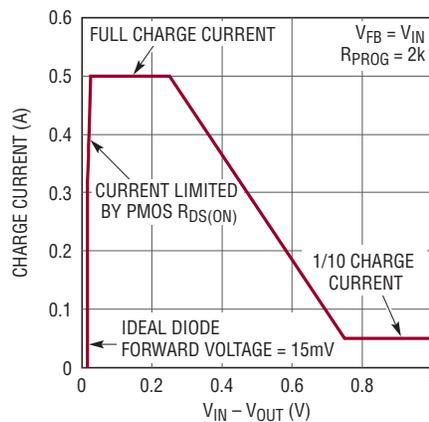

Figure 2. Supercapacitor charge current profile in Normal mode is designed to prevent inrush currents

has an $R_{DS(ON)}$ of approximately 50mΩ, so when $v_{IN} - v_{OUT}$ is small enough, this resistance may limit the current. For $v_{IN} - v_{OUT}$ voltages less than 15mV, the ideal diode shuts off, reducing the current out of v_{OUT} to a small leakage current.

LDO Mode

In LDO mode the regulation function is not controlled by $v_{IN} - v_{OUT}$, but by feedback from the output voltage. LDO mode is chosen by connecting an output voltage divider to the FB pin to set the maximum output voltage. In LDO mode, the LTC4425 behaves like a voltage regulator supplying up the programmed current to the load and to charge the supercapacitor. If the supercapacitor is at the desired voltage, the LTC4425 continues to supply the load current up to the programmed maximum current.

If the desired supercapacitor voltage is as close to v_{IN} as possible, then ground the FB pin. This means that the loop will never reach regulation, but the output voltage

will track the input voltage within 15mV or $I_{V(OUT)} \times R_{DS(ON)}$, whichever is larger.

The LTC4425 limits the current available to the v_{OUT} pin. Usually this current is used to charge the supercapacitor, but could also go to a load. In LDO mode, the current is limited in two ways, the PROG pin, and thermal limiting.

The PROG reference voltage, used in LDO mode, is 1V, and the fraction of the v_{OUT} current that is impressed on the resistor attached to the PROG pin is 1/1000. So the current limit is $1000/R_{PROG}$, and can be as high as 2A.

If one imagines charging a 100F capacitor, even at 2A, the voltage changes at 20mV/s. And, during this charging process there is significant dissipation, usually several watts. If a portion of the v_{OUT} current is going to a system load, then the time to charge the supercapacitor is extended. The LTC4425 has a linear thermal regulation loop that limits the current from v_{OUT}, such that the die temperature remains below 105°C. This is a linear circuit meant for usage under normal operating conditions, not a protection circuit that is only there to prevent damage.

LTC4425 FEATURES

Voltage Clamps

There are voltage clamps on each of the stacked output supercapacitors, from v_{OUT} to v_{MID}, and from v_{MID} to ground. The purpose of these voltage clamps is to ensure that the supercapacitors cannot be charged above their rated voltages. The clamp voltage on each of the

The LTC4425 detects any imbalance in the stacked supercapacitors by comparing V_{MID} to V_{OUT}. When the LTC4425 detects an imbalance, it sinks or sources current from the V_{MID} pin to balance the supercapacitor.

stacked supercapacitors can be selected to be 2.45V or 2.70V, via the SEL pin.

Suppose that the input voltage is 6V, and the FB pin is grounded, so that the LTC4425 is in LDO mode and trying to charge the supercapacitor to the input voltage. The clamps will activate whenever either of the stacked supercapacitors exceed the clamp voltage.

To keep the power dissipation in the clamp circuitry in check, the LTC4425 automatically reduces the charge current to 1/10 of the programmed value whenever either of the stacked supercapacitors approaches the clamp voltage.

Leakage Balancer

The LTC4425 detects any imbalance in the stacked supercapacitors by comparing V_{MID} to V_{OUT}. When the LTC4425 detects an imbalance, it sinks or sources current from the V_{MID} pin to balance the supercapacitor.

The LTC4425 leakage balancer is primarily intended to account for the effects of self, or system leakage, and so the maximum sink or source current is around 1mA. Nevertheless, the interaction of the voltage clamps and leakage balancer will eventually correct even quite large imbalances. The supercapacitor may become unbalanced during charging because one capacitor in the stack is larger or smaller than the other. For the same charge current, the larger capacitor will be a lower voltage than the smaller capacitor. So, the smaller capacitor may activate its voltage clamp before the larger capacitor finishes charging, unbalancing the stack.

Figure 3. Charging 2-cell series supercapacitor from Li-ion source. $\overline{PFO}$ monitors V_{IN} such that power is only switched to the supercap if V_{IN} fails.
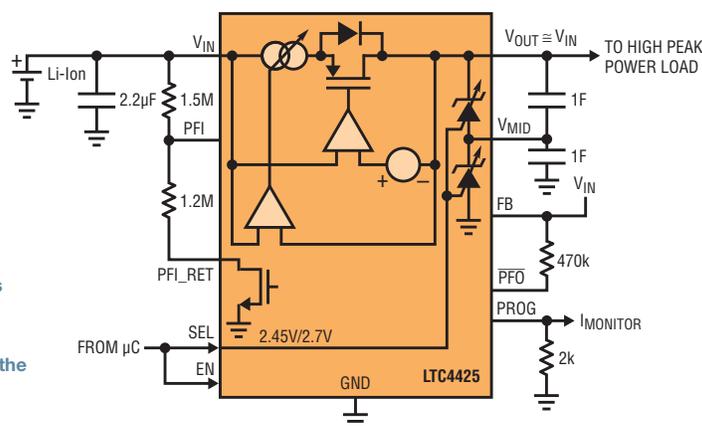
The leakage balancer will then engage and slowly bring the stack back into balance.

$\overline{PFO}$ Output

The LTC4425 monitors and reports conditions of v_{IN} and v_{OUT} depending on the mode. $\overline{PFO}$ goes low if the PFI pin is below 1.2V or ($v_{IN} - v_{OUT}$) > 250mV (in Normal mode) or v_{FB} < 1.11V (in LDO mode), so $\overline{PFO}$ can be used to switch the load to the supercapacitor if there is a loss of v_{IN} (see Figure 3).

This is especially useful if the load current is much higher than the maximum current the LTC4425 can supply. $\overline{PFO}$ can be used to switch the load to the supercapacitor *only* in the absence of v_{IN}.

Note that $\overline{PFO}$ monitors either an input fault, or it indicates a low output voltage at the FB pin. If the FB pin is grounded—that is, setup in LDO mode to charge the supercapacitor to v_{IN}—then $\overline{PFO}$ is permanently asserted low, masking any faults on v_{IN}.

SUPERCAPACITOR-BASED RIDE-THROUGH SYSTEM

Many electronics systems require a short-term power backup system that allows them to ride through brief interruptions in power. In a similar vein, some systems need time to save states, or empty volatile memory or perform other housekeeping tasks when power is abruptly removed. For example, a hard drive may need to park the heads, so that they don't land on the media surface. This is an electromechanical system that requires 20ms–100ms of continuous power before it can completely shut down.

Another example involves the effect of large electrical machines on power systems. If a large electric motor is started, such as a commercial building air conditioner or elevator, the mains supply may collapse for several line cycles. Usually the input supply stores only enough energy for between a half a cycle and one cycle. Devices powered by the input supply need a way to operate normally until the mains recovers.

Supercapacitors are well suited to short-power-burst, ride-through applications.
Their low source impedance allows them to supply significant power for a
relatively short time, and they are considerably more robust than batteries.
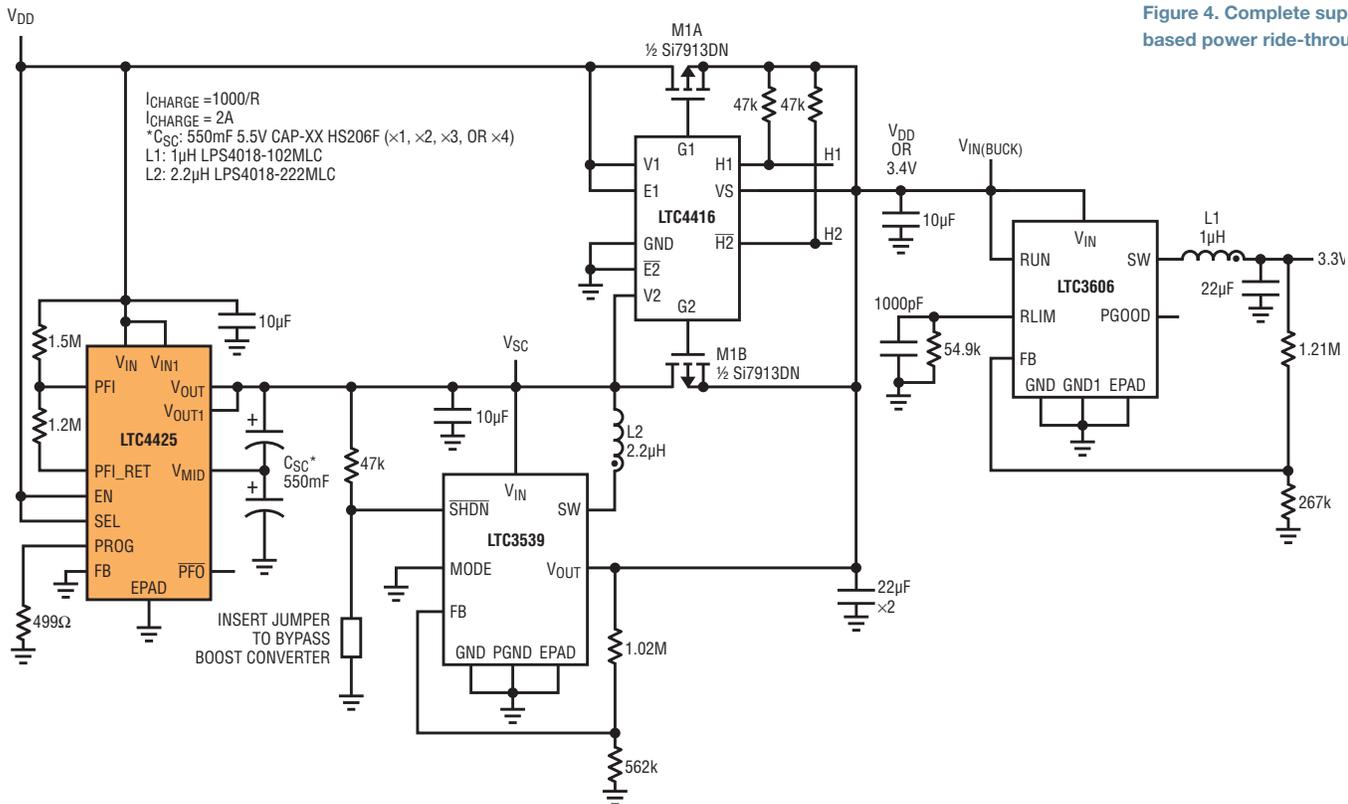
Ride-through applications can certainly be implemented with battery backup, but in many cases, it requires a very large battery array to satisfy the ride-through power requirements. Although batteries can store a lot of energy, they cannot supply much power per volume due to their significant source impedance. Batteries also have relatively short lives, 2~3 years, and their care and feeding requirements are substantial.

Supercapacitors, on the other hand, are well suited to short-power-burst, ride-through applications. Their low source impedance allows them to supply significant power for a relatively

short time, and they are considerably more robust than batteries.

Ride-Through Application Setup
Figure 4 shows a complete power interruption ride-through system using the LTC4425, LTC4416, LTC3539 and LTC3606. Figure 5 shows the layout. This design can hold up a 3.3V rail at 200mA for almost eight seconds.

The LTC3606 is a micropower buck regulator that produces 3.3V. The LTC4416 provides a dual ideal diode-OR function to ensure maximum efficiency when switching from the regular input to the supercap. The LTC3539 is a micropower

boost regulator with output disconnect. This boost regulator operates down to 0.5V, and can support loads of 1.3A × V$_{OUT}$/V$_{IN}$ at its output. The supercapacitor is a CAP-XX HS206F, 0.55F, 5.5V capacitor.

Ride-Through Application Measured Results and Operation Details
Figure 6 shows the waveforms if the LTC3539 boost circuit is disabled. Run time, from input power off to output regulator voltage dropping to 3V, is 4.68s. Figure 7 shows the waveforms if the LTC3539 boost circuit is operational. Run time, from input power off to output regulator dropping to 3V, is 7.92s.

One way to extend the ride-through time for a given supercapacitor is to add a boost regulator to the system, which allows for energy scavenging. The run time of a given supercapacitor can be extended by >30% if energy scavenging is used.

When the LTC3539 boost regulator is disabled, as soon as input power falls, the LTC4416 based ideal diodes switch the input energy supply for the LTC3539 buck regulator to the supercap. In Figure 6, the voltage across the supercap (v_{SC}) linearly decreases due to the constant power load of 200mA at 3.3V on the buck regulator (v_{OUT}).

When the input voltage to the LTC3539 reaches the dropout voltage of the regulator, the output voltage is seen to track the input voltage. At 4.68s after input power removal, the voltage on the supercap reaches 3.0V plus the dropout voltage, and v_{OUT} drops below 3V. The buck regulator continues to track the supercap voltage down until it reaches 2V, whereupon the buck regulator shuts off.

In Figure 7, the voltage across the supercap (v_{SC}) linearly decreases due to the constant power load of 200mA at 3.3V on the buck regulator. When v_{SC} reaches 3.4V, the regulation point of the boost regulator, the boost regulator begins switching. This shuts off the ideal diode and disconnects the buck regulator from the supercapacitor. The energy input to the buck regulator is now the boost regulator's output of 3.4V. v_{SC} remains at 3.4V, but the supercap begins to discharge exponentially, because as the input voltage of the boost regulator drops, it must draw higher and higher current to sustain its output at 3.4V.

Because the input of the buck regulator remains at 3.4V, its output remains in regulation. When the boost regulator reaches its input UVLO it shuts off,
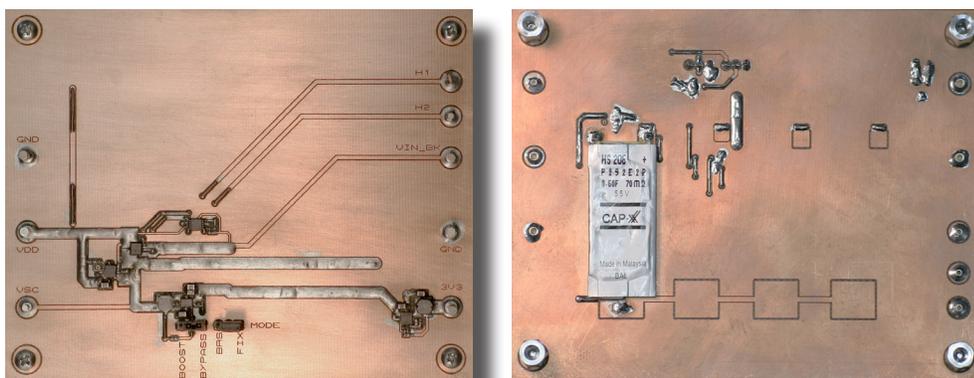
Figure 5. Front and back board layout used to test the circuit in Figure 4

and its output immediately collapses. Since its input voltage has now collapsed, the buck regulator shuts off.

Energy Scavenging in the Ride-Through Application

What voltage should the boost output be set to? Clearly, operation is identical, with or without the boost circuit enabled until the input dropout of the buck regulator is reached. One goal in the design

is to minimize the amount of time that the boost regulator is used in the power chain, because each additional regulation step lowers the overall efficiency. Here, we set the boost regulator output voltage as close to the buck regulator input dropout voltage as possible, or 3.4V.

The boost regulator must have a synchronous output to maximize efficiency once the boost regulator engages. This
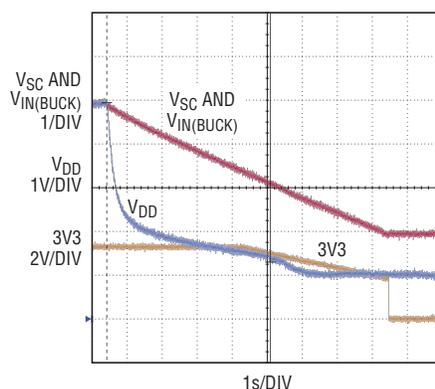
Figure 6. If the boost regulator is disabled in the circuit of Figure 4, the ride-through applications can support a 0.67W load for about 4.68s.
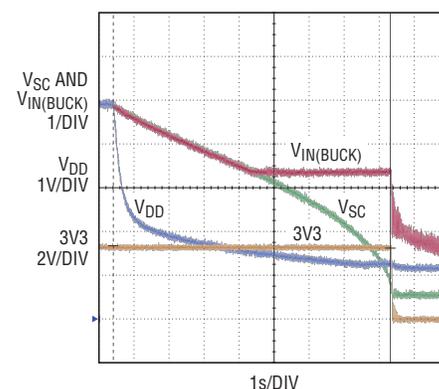

Figure 7. With boost regulator enabled in the circuit of Figure 4, the ride-through applications can support a 0.67W load for about 7.92s.

Ultralow-EMI, 96W, Step-Down µModule Regulator—EN55022 Class B Certified in a 15mm x 15mm Footprint

Richard Ying and Willie Chan

Designers of information technology and communications systems have come face-to-face with the difficult challenge of producing feature-rich, power-hungry products that comply with international EMI standards. Prior to sale, all information technology equipment (ITE)—commonly defined as having a regulated clock signal greater than 9kHz—must meet government standards such as FCC Part 15 Subpart B in the United States, and EN55022 in the European Union. Both standards define maximum allowable radiated emission for industrial and commercial environments (Class A) and home environments (Class B) as shown in Figure 1.

The problem is that the power budgets of ITE products are increasing with performance improvements, so meeting EMI standards becomes proportionally more difficult (see sidebar). Enter the LTM®4613 8A µModule® step-down regulator, which saves significant design time by squeezing guaranteed EMI-compliance and high performance into a single compact package.

EMI RADIATION SOURCES

Electromagnetic waves radiate from any switching converter and its interface leads. Pulsating voltages and currents associated with the switching action of all switch mode converters from ideal sources generate and directly influence the strength of radiated electromagnetic waves. Furthermore, parasitic devices within the converter contribute to electromagnetic radiation. Figure 2 presents a typical buck converter including parasitic inductors and parasitic capacitors of the MOSFETs.

During MOSFET switching, the energy stored in the parasitic inductor resonates with the energy stored in the parasitic capacitor. When the energy is released, the resulting voltage spike at the switch node (v_{SW}) can be as large as twice of the input voltage, as shown in Figure 3. As the current capability of the MOSFET increases, the energy stored in

Electromagnetic Theory and EMI Switch Mode Regulators

A short reflection on electromagnetic theory can help one understand the EMI implications of high current, high power DC/DC step-down converters.

Gauss' law states that the strength of an electric field in a given area over an enclosed volume is proportional to the total charge inside it.

$$\int \bar{E} \cdot d\bar{A} = \frac{q}{\varepsilon_0}$$

Consider this law as applied to a circuit board. A PCB trace is simply a volume of charge, where the amount of charge in it is proportional to the amount of current passing through it (specifically, one ampere equals one coulomb of charge per second.) So, higher currents create stronger electric fields.

Additionally, in a switch mode regulator, these fields vary in strength as currents change throughout the switching cycle. Maxwell's equations tell us that a constantly varying electric field creates a self-sustaining electromagnetic wave.

If currents change rapidly, as is the case in a switch mode regulator, some of the electromagnetic energy is radiated into the environment, which can cause electromagnetic interference (EMI). EMI is produced by all of the current loops within a step-down regulator. In general, EMI mitigation becomes increasingly important, and difficult, as power consumption goes up.

While this short description is incomplete, leaving out, for example, the implications of the magnetic component surrounding the current paths and the rapid polarity changes on the inductor, it shows the relationship between a regulator's increasing output power and radiated EMI, which must be addressed with good design practices.

Figure 1. FCC radiated limits (USA) and EN55022 class B radiated limit (European Union)
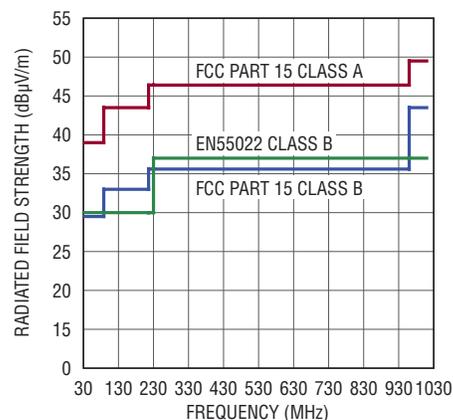
Figure 2. Buck switching regulator with parasitic inductor and capacitors
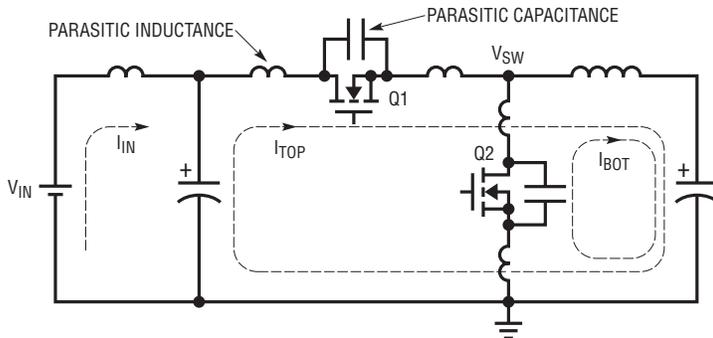

Figure 3. Typical switch node voltage spike and ringing in a 12V input buck switching regulator
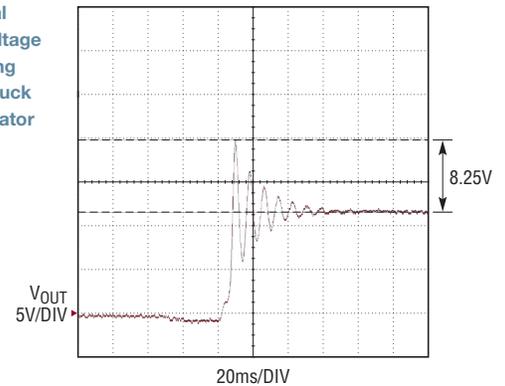
the parasitic capacitor tends to increase as well. The switching action also pulses the input current and the current flowing through both top MOSFET (I_{TOP}) and bottom MOSFET (I_{BOT}). This pulsating current generates electrical waves on the input supply cable and on the PCB board traces, which act as transmitting antennae.

The magnitude of the voltage spike at the switching node increases as input voltages and output currents increase. Likewise,

the higher the output current, the larger the pulsating current generated inside the circuit loop. In the end, radiated emission is highly dependent on the operating condition of the device, so testing should take into account worst-case conditions. In general, radiated EMI increases with higher input voltage and higher output power, particularly output current.

Linear regulators are the usual go-to, low-EMI alternative to switching regulators, but power levels and input voltages have reached a point where linear regulators produce too much heat to be practical. Design engineers are thus forced to overcome the EMI challenges of switching regulators in order to meet the performance requirements of today's equipment.

EMI MITIGATION

There are several ways to reduce the radiated emissions from a switch mode power converter design. One conventional method is to surround the entire power solution with an EMI shield, essentially

containing the EMI field within a metal enclosure. The obvious problem is that a metal box adds significant complexity, size and cost. Alternatively, an RC snubber circuit at the switching node (v_{SW}) can reduce the voltage spike and subsequent ringing, but adding an RC snubber circuit significantly reduces operating efficiency. Finally, careful PCB layout,

Figure 4. Demonstrated EN55022 compliance LTM4613 (DC1743) at 96W as conducted by independent tests
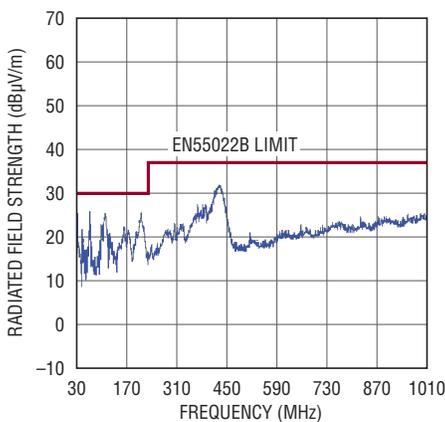
**Figure 5. Radiated emission test setup**
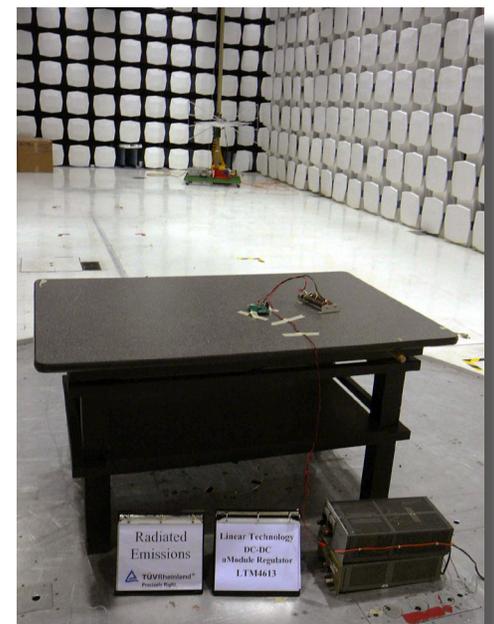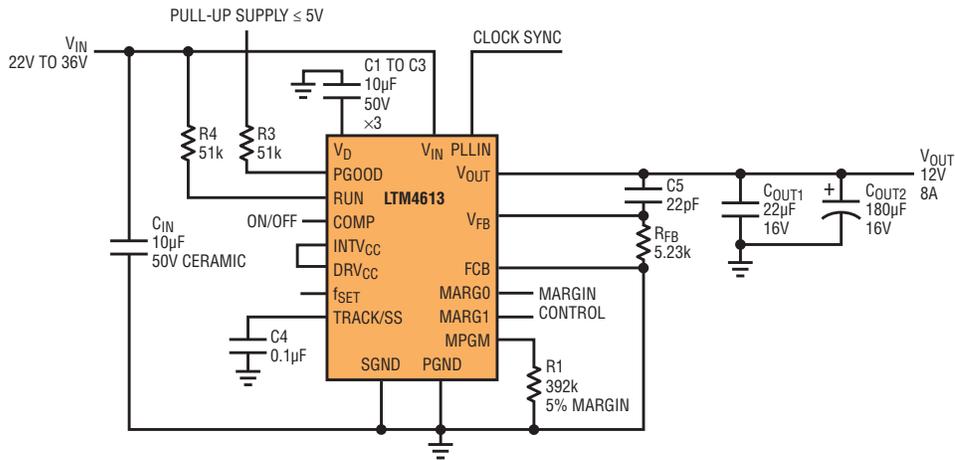
Figure 6. LTM4613 12V/8A output application circuit
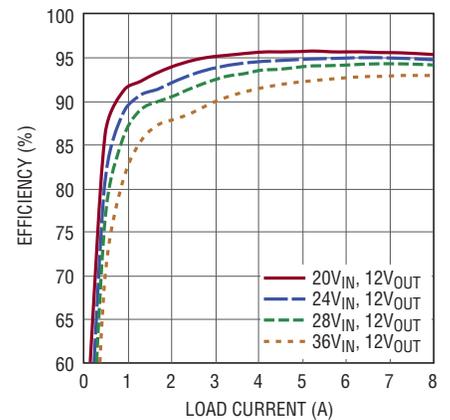
Figure 7. LTM4613 efficiency vs load current with 12V output

such as using local low ESR ceramic decoupling capacitors and minimizing PCB trace distances for high current paths, can reduce the parasitic inductance as shown in Figure 2 and help reduce EMI.

Overall, a power engineer must apply years of experience to evaluate tough trade-offs when designing a power supply that meets stringent size, efficiency, heat and EMI specifications, especially in high input voltage, high output power applications. Often, a huge amount of time and energy are spent evaluating the trade-offs inherent in designing an EMI-compliant power converter.

Ideally, extensive design experience and best practices could be prepackaged into a converter that complies with EMI standards while minimizing performance trade-offs. Fortunately, that ideal is achieved by the LTM4613.

GUARANTEED EMI COMPLIANCE

The LTM4613 8A µModule step-down regulator is certified by an independent test laboratory, TUV Rheinland, to meet EN55022 Class B EMI emissions limits at up to 96W of output power (Figure 4). TUV Rheinland is ISO 17025

accredited by the U.S. National Institute of Standards and Technology (NIST) in North America and the Notified Bodies on the European Union, the most meticulous and recognized certifying labs in the industry. Figure 5 shows a complete radiated emissions 30MHz to 1000MHz test setup using the standard LTM4613 demonstration board (DC1743) in TUV Rheinland's 10-meter semi-anechoic chamber as specified by EN55022.

EMI compliance is worthless if the regulator can't meet other stringent space and performance requirements. That's where the LTM4613 excels. This nearly complete converter comes in a space-saving 15mm × 15mm package that requires only input capacitance, output capacitance, and a few other small components to make a step-down regulator. Performance is optimized to minimize power dissipation, maximize efficiency and assure tight regulation. The LTM4613 accepts input voltages from 5V to 36V and delivers a regulated output voltage from 3.3V to 15V with 2.0% maximum total DC error over line, load and temperature. A 24V input to 12V output conversion reaches peak operating efficiencies of around 95%.

CONCLUSION

The LTM4613 delivers high output power and efficiency with demonstrated EMI performance that complies with EN55022 Class B. With carefully designed integrated filter, meticulous internal layout, shielded inductor, internal snubber circuitry and power transistor driver, the LTM4613 achieves a perfect balance between the size, output power, efficiency and emission. The LTM4613 eliminates the need for external filters, magnetic shields, and ferrite beads for a trouble-free design process, making it easy to design safe, EMI-compliant power supplies.

When comparing products, be certain the EN55022 certification was performed under similar conditions, as EMI field strength and the ability to pass EMI regulations is highly dependent on factors such as the input voltage, output current, output voltage and PCB layout. All LTM4613 test operating conditions and design files are freely available. Designers using the LTM4613 can be confident that it will perform as certified. ■

UMTS Base Station Receiver Fits in Half-Inch Square

Douglas Stuetzle and Todd Nelson

How much integration is possible while still meeting macrocell base station performance requirements? Process technology dictates that certain key functions are produced in specific processes: GaAs and SiGe in the RF realm, fine-line CMOS for high speed ADCs, and high-Q filters cannot be implemented well in semiconductor materials. Yet the market continues to demand higher integration.

With that in mind, Linear Technology has applied system-in-package (SiP) technology to build a receiver occupying about one-half square inch (just over 3cm²). The boundaries of the receiver are the 50Ω RF input, the 50Ω LO input, the ADC clock input and the digital ADC output. This leaves the low noise amplifier (LNA) and RF filtering to be added for the input, LO and clock generation, and digital processing of the digital output. Within the 15mm × 22mm package is a signal chain utilizing SiGe high

frequency components, discrete passive filtering and fine-line CMOS ADCs.

This article presents a design analysis for the LTM9004 µModule® receiver implementing a direct conversion receiver.

DESIGN TARGETS

The design target is a Universal Mobile Telecommunications System (UMTS) uplink Frequency Division Duplex (FDD) system specifically the Medium Area Base Station in Operating Band I as detailed in the 3GPP TS25.104 v7.4.0 specification. Sensitivity is a primary

consideration for the receiver; the requirement is ≤(–111dBm), for an input SNR of –19.8dB/5MHz. That means the effective noise floor at the receiver input must be ≤(–158.2dBm/Hz).

DESIGN ANALYSIS: ZERO-IF OR DIRECT CONVERSION RECEIVER

The LTM®9004 is a direct conversion receiver utilizing an I/Q demodulator, baseband amplifiers and a dual 14-bit, 125Msps ADC as shown in Figure 1. The LTM9004-AC lowpass filter has a 0.2dB corner at 9.42MHz, allowing four WCDMA carriers. The LTM9004 can be used with an RF front end to build a complete UMTS band uplink receiver. An RF front end consists of a diplexer, along with one or more low noise amplifiers (LNAs) and ceramic bandpass filters. To minimize gain and phase imbalance, the baseband chain implements a fixed gain topology, so an RF VGA is required preceding the

Figure 1. Direct conversion architecture implemented in the LTM9004 µModule receiver

LTM9004. Here is an example of typical performance for such a front end:

- Rx frequency range: 1920 to 1980MHz

- RF gain: 15dB maximum

- AGC range: 20dB

- noise figure: 1.6dB

- IIP2: +50dBm

- IIP3: 0dBm

- P_{1dB}: −9.5dBm

- rejection at 20MHz: 2dB

- rejection at Tx band: 96dB

Given the effective noise contribution of the RF front end, the maximum allowable noise due to the LTM9004 must then be −142.2dBm/Hz. Typical input noise for the LTM9004 is −148.3dBm/Hz, which translates to a calculated system sensitivity of −116.7dBm.

Typically, such a receiver enjoys the benefits of some DSP filtering of the digitized signal after the ADC. In this case, assume the DSP filter is a 64-tap RRC lowpass with alpha equal to 0.22. To operate in the presence of co-channel interfering signals, the receiver must have sufficient dynamic range at maximum sensitivity. The UMTS specification calls for a maximum co-channel interferer of −73dBm. Note the input level for −1dBFS within the IF passband of the LTM9004 is −15.1dBm for a modulated signal with a 10dB crest factor. At the LTM9004 input this amounts to −53dBm, or a digitized signal level of −2.6dBFS.
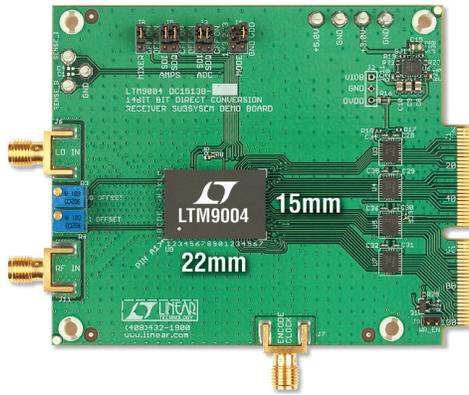

Figure 2. Minimal external required circuitry is required to build a complete receiver

With the RF automatic gain control (AGC) set for minimum gain, the receiver must be able to demodulate the largest anticipated desired signal from the handset. This requirement ultimately sets the maximum signal the LTM9004 must accommodate at or below −1dBFS. The minimum path loss called out in the specification is 53dB, and assumes a handset average power of +28dBm. The maximum signal level is then −25dBm at the receiver input. This is equivalent to −14.6dBFS peak.
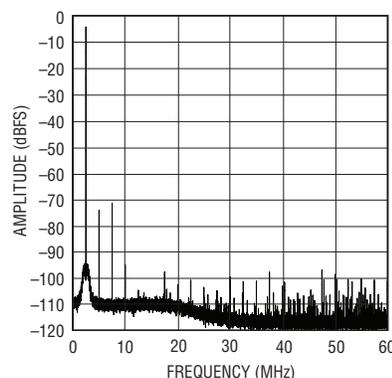
There are several blocker signals detailed in the UMTS system specification. Only a specified amount of desensitization is allowed in the presence of these signals—the sensitivity specification is −115dBm. The first of these is an adjacent channel 5MHz away, at a level of −42dBm. The level of the digitized signal is −11.6dBFS peak. The DSP post-processing adds 51dB rejection, so this signal is equivalent to an interferer at −93dBm at the input of the receiver. The resulting sensitivity is −112.8dBm.

The receiver must also contend with a −35dBm interfering channel ≥10MHz away. The IF rejection of the μModule receiver will attenuate it to an equivalent digitized signal level of −6.6dBFS peak. With the DSP post-processing it amounts to −89.5dBm at the receiver input and the resulting sensitivity is −109.2dBm.

Out-of-band blockers must also be accommodated, but these are at the same level as the in-band blockers which have already been addressed.

Figure 3. Single tone FFT

Figure 4. Baseband frequency response
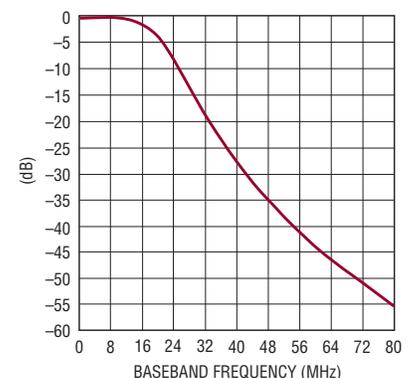
The LTM9004 can be used with an RF front end to build a complete UMTS band uplink receiver.

In all of these cases, the typical input level for −1dBFS of the LTM9004 is well above the maximum anticipated signal levels. Note that the crest factor for the modulated channels will be on the order of 10dB–12dB, so the largest of these will reach a peak power of approximately −6.5dBFS at the LTM9004 output.

The largest blocking signal is the −15dBm CW tone ≥20MHz beyond the receive band edges. The RF front end will offer 37dB rejection of this tone, so it will appear at the input of the LTM9004 at −32dBm. Here again, a signal at this level must not desensitize the baseband µModule receiver. The equivalent digitized level is only −41.6dBFS peak, so there is no effect on sensitivity.

Another source of undesired signal power is leakage from the transmitter. Since this is an FDD application, the receiver described here will be coupled with a transmitter operating simultaneously. The transmitter output level is assumed to be ≤(+38dBm), with a transmit to receive isolation of 95dB. Leakage appearing at the LTM9004 input is then −31.5dBm, offset from the receive signal by at least 130MHz. The equivalent digitized level is only −76.6dBFS peak, so there is no desensitization.

One challenge of direct conversion architectures is 2nd order linearity. Insufficient 2nd order linearity allows any signal, wanted or unwanted, to create DC offset or pseudo-random noise at baseband. The blocking signals detailed above will then degrade sensitivity if this

pseudo-random noise approaches the noise level of the receiver. The system specification allows for sensitivity degradation in the presence of these blockers in each case. Per the system specification, the −35dBm blocking channel may degrade sensitivity to −105dBm. As we have seen above, this blocker constitutes an interferer at −15dBm at the receiver input. The 2nd order distortion produced by the LTM9004 input is about 16dB below the thermal noise, and the resulting predicted sensitivity is −116.6dBm.

The −15dBm CW blocker also gives rise to a 2nd order product; in this case the product is a DC offset. DC offset is undesirable, as it reduces the maximum signal the A/D converter can process. The one sure way to alleviate the effects of DC offset is to ensure the 2nd order linearity of the baseband µModule receiver is high enough. The predicted DC offset due to this signal is <1mV at the input of the ADC.

Note that the transmitter leakage is not included in the system specification, so the sensitivity degradation due to this signal must be held to a minimum. The transmitter output level is assumed to be ≤(+38dBm), with a transmit to receive isolation of 95dB. The 2nd order distortion generated in the LTM9004 is such that the loss of sensitivity is <0.1dB.

There is only one requirement for 3rd order linearity in the specification. In the presence of two interferers, the sensitivity must not degrade below −115dBm. The interferers are a CW tone and a WCDMA channel at −48dBm each.

These appear at the LTM9004 input at −28dBm each. Their frequencies are such that they are 10MHz and 20MHz away from the desired channel, so the 3rd order intermodulation product falls at baseband. Here again, this product appears as pseudo-random noise and thus reduces the signal to noise ratio. The 3rd order distortion produced in the LTM9004 is about 20dB below the thermal noise floor, and the predicted sensitivity degradation is <0.1dB.

MEASURED PERFORMANCE

Using the evaluation boards shown in Figure 2, the LTM9004-AC achieved excellent results as shown in Figures 3 and 4. The test setup consisted of two Rohde & Schwarz SMA 100A signal generators for RF and LO, a Rohde & Schwarz SMY 01 generator for the ADC clock and TTE inline filters.

The LTM9004-AC consumes a total of 1.83 W from 5V and 3V supplies. AC performance includes SNR of 72dB/9.42MHz and SFDR of 66dB.

CONCLUSION

The LTM9004 exhibits the high performance necessary for UMTS base station applications, yet offers the small size and integration necessary for very compact designs. By utilizing SiP technology, the µModule receiver utilizes components made on optimum processes (SiGe, CMOS) and passive filter elements. ∎

What's New with LTspice IV?

Gabino Alonso

NEW HOW-TO VIDEOS

Using Transformers in LTspice® IV
video.linear.com/93

Transformers and coupled inductors are key components in many switching regulator designs, including flyback, forward and SEPIC converters. Although it is possible to make a dedicated subcircuit for a specific transformer, it is often better in LTspice IV to define a separate inductor for each transformer winding, and then couple them all together magnetically via a single mutual inductance (κ) statement. This video shows how to define a transformer using inductors and specify the mutual inductance via a single κ statement in your LTspice IV simulations.

Two new LTspice IV how-to videos are now available

Transformers

3rd-Party Models

What is LTspice IV?

LTspice® IV is a high performance SPICE simulator, schematic capture and waveform viewer specifically designed to speed up the process of power supply design. LTspice IV adds enhancements and models to SPICE, significantly reducing simulation time compared to typical SPICE simulators, allowing one to view waveforms for most switching regulators in minutes compared to hours for other SPICE simulators.

LTspice IV is available free from Linear Technology at www.linear.com/LTspice. Included in the download is a complete working version of LTspice IV, macro models for Linear Technology's power products, over 200 op amp models, as well as models for resistors, transistors and MOSFETs.

Adding Third-Party Models to LTspice IV
video.linear.com/97

LTspice IV includes models for many discrete components, such as transistors and MOSFETs, but many component manufacturers make additional models that you can add to your LTspice IV circuit simulations. These third-party SPICE models are described in .MODEL and .SUBCKT statements. This video provides an overview of how to add a third-party .MODEL statement for an intrinsic SPICE device and how to add and create a symbol for a third party .SUBCKT statement.

NEW LTspice DEVICE MACRO MODELS

To update your installation of LTspice IV with the latest models, choose Sync Release from the Tools menu. You can review the changelog.txt after Sync Release for the complete list of new models. Here is a list of some new models:

µModule Regulators
- **LTM8048:** 3.1V to 32V input isolated µModule DC/DC converter with LDO post regulator www.linear.com/8048

- **LTM8047:** 3.1V to 32V isolated µModule DC/DC converter www.linear.com/8047

Switching Regulators
- **LTC3765:** Active clamp forward controller and gate driver www.linear.com/3765

- **LTC3766:** High efficiency, secondary-side synchronous forward controller www.linear.com/3766

- **LT®3759:** Wide input voltage range boost/SEPIC/inverting controller www.linear.com/3759

- **LTC3536:** 1A low noise, buck-boost DC/DC converter www.linear.com/3536

- **LT3507A:** Triple monolithic step-down regulator with LDO www.linear.com/3507A

Linear Regulators
- **LT3015:** 1.5A, low noise, negative linear regulator with precision current limit www.linear.com/3015

Amplifiers & Comparators
- **LT6108:** High side current sense amplifier with reference and comparator www.linear.com/6108

- **LTC6360:** Very low noise single-ended SAR ADC driver with true zero output www.linear.com/6360
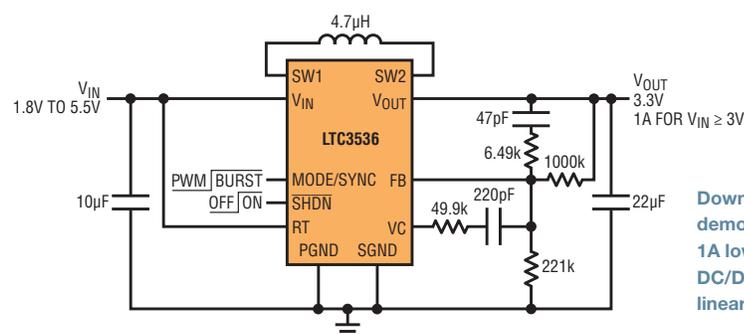
Download the LTspice IV demonstration circuit for this 1A low noise, buck-boost DC/DC converter at www.linear.com/3536

HOW TO USE THE .STEP COMMAND TO PERFORM REPEATED ANALYSIS

There are two ways to examine a circuit by changing the value for a particular parameter: you can either manually enter each value and then resimulate the circuit to view the response, or use the .step command to sweep across a range of values in a single simulation run.

The .step command causes an analysis to be repeatedly performed while stepping through a model parameter, global parameter or independent source. Here is an example waveform response of an RC circuit, for which the capacitance is stepped through three values.

To implement this in LTspice IV, perform the following steps:

Define the component parameter with a variable by editing the component attribute (Ctrl–right-click on the component) and entering "{X}" for the

Value, where "X" is a user defined variable name. The addition of the curly braces around the variable is important as it tells LTspice IV that "X" is a parameter.

Add a .step command via a SPICE directive that specifies the steps for the parameter "X" by a linear, logarithmic or list of values.

Example A: ".step param X list .1u .2u .3u" steps the parameter X through each value listed.

Example B: ".step param X .1u .3u .1u" steps the parameter X from 0.1u to 0.3u in 0.1u increments.

For more information on how to use the .step command to improve your understanding of a schematic, review the Help Topics in LTspice IV.

Happy simulations!
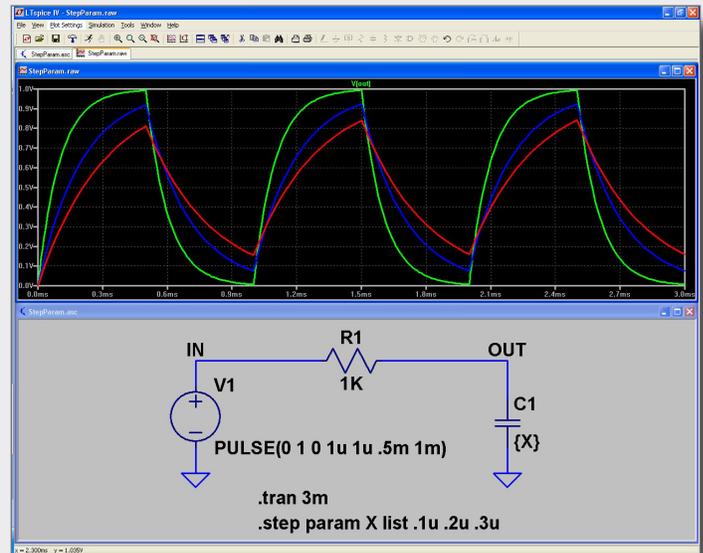
NEW LTspice IV DEMO CIRCUITS

The LTspice IV circuit collection is available at www.linear.com/DemoCircuits. Here are some of the new demonstration circuits now available:

Switching Regulators

- **LTC3618:** Dual monolithic synchronous step-down converter for DDR termination (2.25V–5.5V to V$_{DDQ}$ at ±3A, VTTR at ±10mA, VTT at ±3A) www.linear.com/3618

- **LTC3617:** Monolithic synchronous step-down regulator for DDR termination (2.25-5.5V to VTTR at 10mA, VTT at ±6A) www.linear.com/3617

- **LTC3536:** 1A low noise, buck-boost DC/DC converter (1.8V–5.5V to 3.3V at 1.0A) www.linear.com/3536

Battery Charger

- **LT3652:** 1A solar-panel-powered 3-stage 12V lead-acid fast/float charger (10V–16V to 12V at 1A) www.linear.com/3652
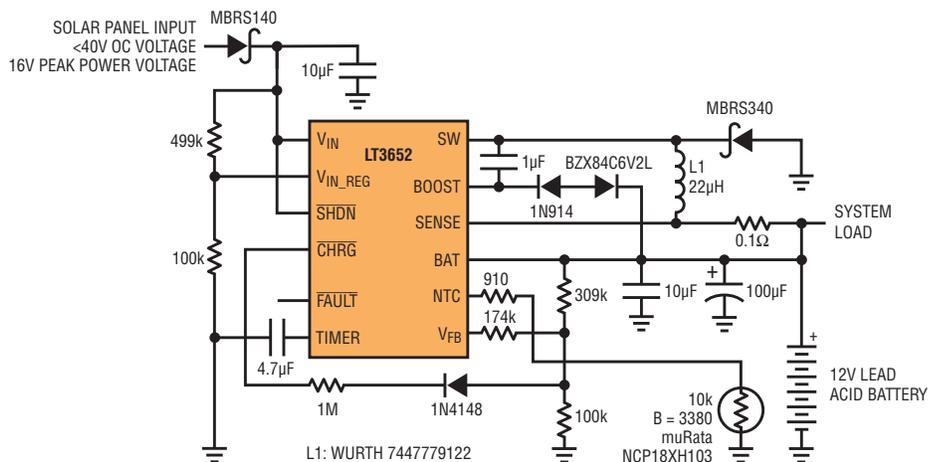
The LTspice IV demonstration circuit for this 1A solar-panel-powered 3-stage 12V lead-acid fast/float charger is available at **www.linear.com/3652**

Linear Regulators

- **LT3032:** Dual 150mA Positive/Negative Low Noise LDO Linear Regulator (5V to 3.3V at 0.15A & −5V to −3.3V at 0.15A) www.linear.com/3032

- **LT3029:** Dual 500mA/500mA LDO, low noise, μpower linear regulator (3V to 1.8V at 0.5A & 3V to 1.5V at 0.5A) www.linear.com/3029

- **LT3015:** 1.5A, low noise, negative linear regulator with precision current limit (−7V to −5.0V at −1.5A) www.linear.com/3015 ∎
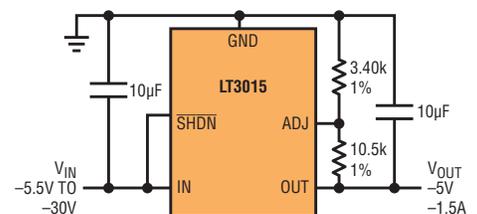
The demonstration circuit for this 1.5A, low noise, negative linear regulator with precision current limit is available at **www.linear.com/3015**

System Monitor with Instrumentation-Grade Accuracy Used to Measure Relative Humidity

Leo Chen

The LTC2991 is designed to measure supply voltages, currents and temperatures on large circuit boards when used in system monitor applications. It is also capable of delivering ±1°C accuracy when using a 1-cent MMBT3904 transistor as a temperature sensor, making it suitable for many instrumentation applications. Temperature is the most measured physical parameter, with sensor selection a function of accuracy requirements, durability, cost and compatibility with the medium being measured. An inexpensive NPN transistor is an ideal sensor for applications calling for disposable sensors, or those that require a large number of sensors.

A PSYCHROMETER: NOT NEARLY AS OMINOUS AS IT SOUNDS

A psychrometer is a type of hygrometer, a device that measures relative humidity. It uses two thermometers, one dry (dry bulb) and one covered in a fabric saturated with distilled water (wet bulb). Air is passed over both thermometers, either by a fan or by swinging the instrument, as in a "sling psychrometer." A psychrometric chart is then used to calculate humidity from the dry and wet bulb temperatures. Alternatively, a number of equations exist for this purpose. The following equations are used in testing this circuit.

WET = wet bulb temperature in Celcius
DRY = dry bulb temperature in Celcius
P = pressure in kPa

$$A = 6.6 \bullet 10^{-4} \bullet \left(1 + 1.115 \bullet 10^{-3} \bullet WET\right)$$

$$ESWB = e^{\left(\frac{16.78 \bullet WET - 116.9}{WET + 273.3}\right)}$$

$$ED = ESWB - A \bullet P \bullet (DRY - WET)$$

$$EDSB = e^{\left(\frac{16.78 \bullet DRY - 116.9}{DRY + 273.3}\right)}$$

$$HUMIDITY = \frac{ED}{EDSB}$$

Figure 1 shows the LTC2991-based psychrometer. The two transistors provide the wet bulb and dry bulb temperature readings when connected to the appropriate inputs of the LTC2991.

The equations include atmospheric pressure as a variable, which is determined here via a Novasensor NPP301-100

Figure 1. Simple psychrometer using the LTC2991
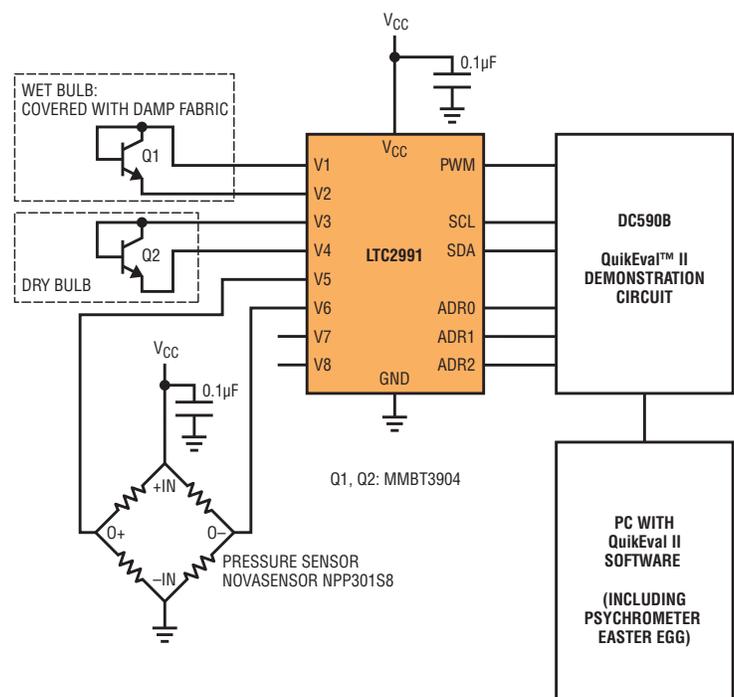
An inexpensive NPN transistor is an ideal temperature sensor for applications calling for disposable sensors, or those that require a large number of sensors.

barometric pressure sensor measured by channel x configured for a differential input. Full-scale output is 20mV per volt of excitation voltage, at 100kPa barometric pressure (pressure at sea level is approximately 101.325kPa).

The LTC2991 can also measure its own supply voltage (which in our circuit is the same supply rail used to excite the pressure sensor). Thus it is easy to calculate a ratiometric result from the pressure sensor, removing the error contribution of the excitation voltage.

ERROR BUDGET

The LTC2991 remote temperature measurements are guaranteed to be accurate to ±1°C. Figure 2 shows the error in indicated humidity that results from a 0.7°C error in the worst-case direction, and the error in indicated humidity that results from a 0.7°C error in the worst-case direction combined with worst-case error from the pressure sensor. This error falls within the range of accuracy of the psychrometric equations themselves. Should higher accuracy be required, a lookup table with the psychrometric charts would need to be implemented.
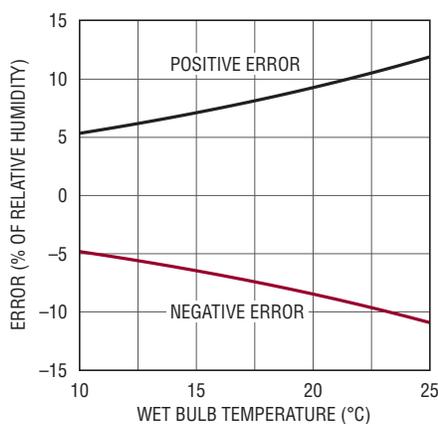

Figure 2. Worst-case error

TRY IT OUT!

A psychrometer readout is implemented as an Easter egg in the LTC2991 (DC1785A) demonstration software, available as part of the Linear Technology QuikEval™ software suite.

The demo board should be connected as shown in Figure 1. To access the readout, simply add a file named "tester. txt" (without the quotes) in the install directory of your DC1785A software. The contents of this file do not matter. On software start-up, the message "Test mode enabled" should be shown in the status bar, and a Humidity option will appear in the Tools menu. Relative humidity readings can then be compared to sensors of similar accuracy grade, such as resistive and capacitive film. ∎

Figure 3. A psychrometer readout is implemented as an Easter egg in the LTC2991 (DC1785A) demonstration software, available as part of Linear's QuikEval software suite.
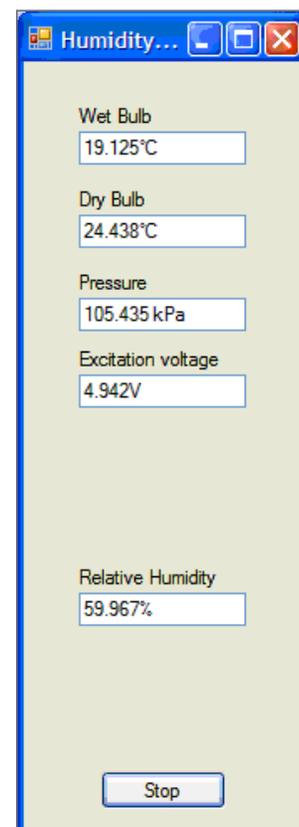
Negative Voltage Diode-OR Controller Tolerates Inputs to 300V and Beyond

Mitchell Lee

The LTC4354 negative voltage diode-OR controller is designed to operate with inputs of up to 100V. As shown in Figure 1, the maximum voltage between –48V, V_A and –48V, V_B is limited to 100V, and the voltage applied to either input is similarly limited to 100V relative to –48COM. A careful study of the LTC4354 data sheet reveals that the drain pins, DA and DB, which are the only pins exposed to high voltage, are limited to 80V. Nevertheless, with a 2k series limiting resistor, these pins can handle up to 100V.

Figure 1. The LTC4354 shown in a 10A,–48V application handles up to 100V differential across the inputs

*REQUIRED TO SUPPRESS PARASITIC OSCILLATIONS IN M1 AND M2. **DO NOT OMIT.**
M1, M2: FAIRCHILD FDMS86101
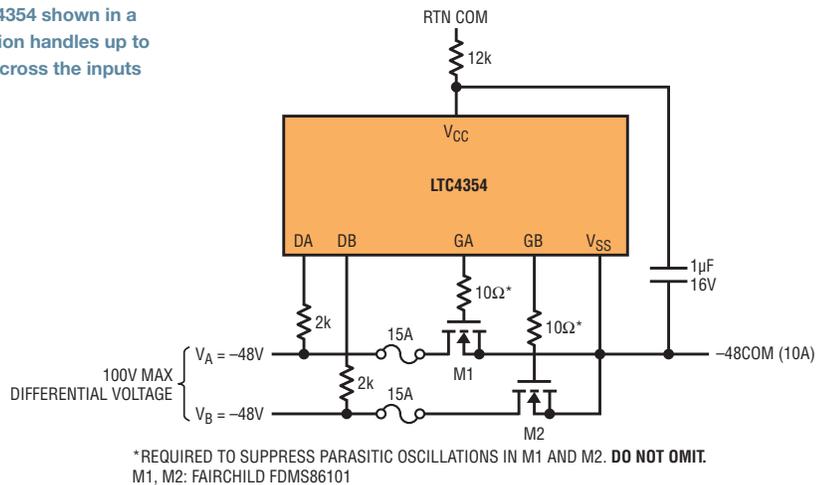
If it were possible to further increase the series resistance, even higher voltages could be tolerated by simply changing the 2k resistor. Unfortunately the drain pin input bias current sets a practical limit of 2k, so as to avoid interfering with the operation of the ideal diode function itself.

In systems where the inputs are subjected to spikes in excess of 100V, MOSFET breakdown clamps the maximum voltage, although admittedly bereft of characterization and guarantee.

If spikes in excess of 100V are an issue, the high voltage capability of the drain pins is easily extended beyond 100V by simply adding a Zener clamp, as shown in Figure 2. Input spikes above 75V are clamped by the Zener, with current limiting provided by the 2k resistor.

Zeners in the 250mW to 500mW range are capable of absorbing the peak current generated by a 150V, 10µs spike. Higher voltage and longer duration spikes may be accommodated by larger devices.

For sustained conditions, a simple Zener clamp is made untenable by the dissipation in both the resistor and Zener. The circuit shown in Figure 3 uses small, high voltage MOSFETs for limiting and can handle up to 400V. 11V gate

Figure 2. Zener clamps extend transient voltage capability to 150V and beyond
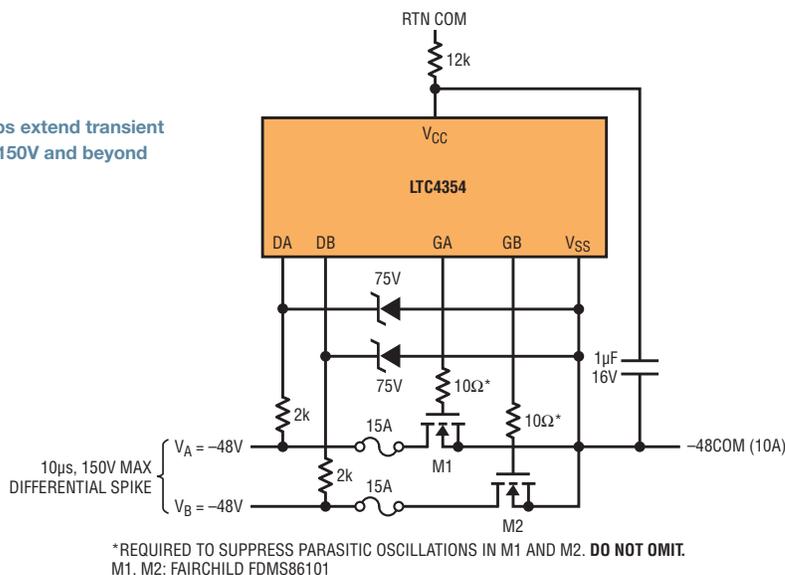
*REQUIRED TO SUPPRESS PARASITIC OSCILLATIONS IN M1 AND M2. **DO NOT OMIT.**
M1, M2: FAIRCHILD FDMS86101

Zeners in the 250mW to 500mW range are capable of absorbing the peak current generated by a 150V, 10µs spike. Higher voltage and longer duration spikes may be accommodated by larger devices.

bias is conveniently obtained from the shunt-regulated v_{CC} pin without the need for any extra components, making this useful configuration a very simple modification of the basic circuit.

Under normal conditions, the –48V inputs are at or near the v_{SS} potential, and the small MOSFETs M3 and M4 are driven fully on as their gates are biased to ~11V with respect to v_{SS} by the v_{CC} pin. If one input rises with respect to v_{SS}, the small MOSFET remains on and the associated drain pin tracks the input. If the input continues to rise to the point where it is ≥10V with respect to v_{SS}, the small MOSFET turns into a source follower, safely limiting the drain pin to about 10V with respect to v_{SS}. MOSFETs

M1 and M2 can be expected to avalanche and clamp any positive-going spikes exceeding 300V, to less than 400V.

While the circuit in Figure 3 was designed for a –48V system, changing R_{IN} to a 100k, 1W unit allows the circuit to operate with inputs of –200V to –300V DC. Higher voltage standoff is possible with appropriate selection of MOSFETs. ∎


Figure 3. The LTC4354 shown in a 10A,–48V application handles up to 300V differential across the inputs

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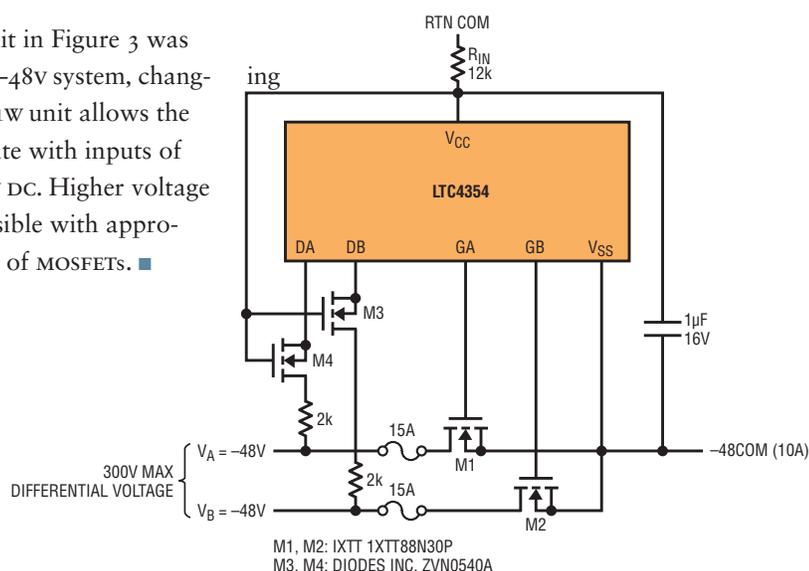
implies a boost regulator with a "blocking" output. This in turn necessitates the second ideal diode to allow the supercapacitor to power the buck regulator until the boost regulator engages. The boost regulator must operate to as low a voltage as possible to ensure that the maximum amount of energy is scavenged from the supercapacitor.

If the supercapacitor is initially charged to 5V, then the energy in the supercapacitor is:

$$\frac{1}{2}CV^2 = \frac{1}{2}0.55F \cdot 5^2 = 6.875J$$

The output power is 3.33V at 0.2A = 0.67W, so the percentage of the energy stored in the supercap that is extracted with a buck-only circuit is:

$$\frac{\varepsilon_{LOAD}}{\varepsilon_{CAP}} = \frac{0.67 \cdot 4.68s}{6.875} = 45.1\%$$

The percentage of the energy stored in the supercap, extracted when the boost regulator is enabled, is:

$$\frac{\varepsilon_{LOAD}}{\varepsilon_{CAP}} = \frac{0.67 \cdot 7.92s}{6.875} = 77\%$$

The percentage of energy stored in the supercapacitor that is recovered increases from 45.1% to 77%. This allows use of a smaller, less expensive supercapacitor.

CONCLUSION
The power ride-through system shown here uses a 0.55F supercap to hold up power long enough for a microcontroller to complete some last gasp housekeeping tasks. One way to extend

the ride-through time for a given supercapacitor is to add a boost regulator to the system, which allows for energy scavenging. The run time of a given supercapacitor can be extended by >30% if energy scavenging is used. This is particularly relevant if the supercapacitor operating voltage is reduced to ensure high temperature reliability.

In addition, the shape of the output voltage is considerably improved as the input voltage to the output regulator is now square in shape. This results in a steady 3.3V output voltage with a sharp cutoff, instead of a ramped voltage drop as the supercap drains. ∎

DUAL BATTERY LOAD SHARING WITH AUTOMATIC SWITCHOVER TO A WALL ADAPTER

The LTC4415 contains two monolithic PowerPath™ ideal diodes, each capable of supplying up to 4A with typical forward conduction resistance of 50mΩ. The diode voltage drops are regulated to 15mV during forward conduction at low currents, extending the power supply operating range and ensuring no oscillations during supply switchover. Less than 1µA of reverse current flows from OUT to IN making this device well suited for power supply ORing applications.

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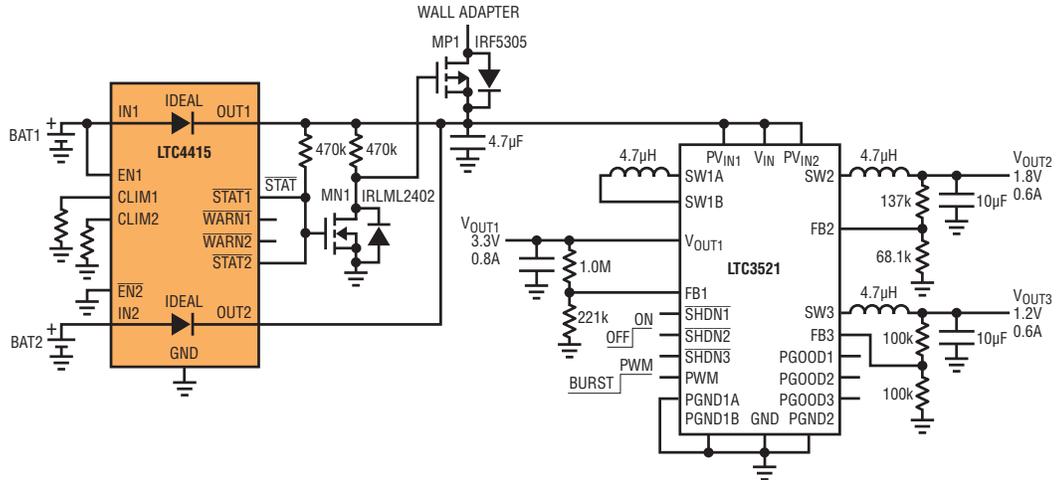
SIMPLE BIDIRECTIONAL DC MOTOR SPEED CONTROLLER WITHOUT A TACHOMETER

Here is one approach for motor speed control without using a tachometer. Using the enable feature of the LT1970A, the drive to the motor can be removed periodically. With no drive applied, the spinning motor presents a back EMF voltage proportional to its rotational speed. The LT1782 is a tiny rail-to-rail amplifier with a shutdown pin. The amplifier is enabled during this interval to sample the back EMF voltage across the motor. This voltage is then buffered by one-half of an LT1638 dual op amp and used to provide the feedback to the LT1970A integrator. When re-enabled the LT1970A will adjust the drive to the motor until the speed feedback voltage, compared to the speed-set input voltage, settles the output to a fixed value. A 0V to 5V signal for the motor speed input controls both rotational speed and direction. The other half of the LT1638 is used as a simple pulse oscillator to control the periodic sampling of the motor back EMF.

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